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CONTROL – DISPLAY INTEGRATION PROGRAM

AFFDL-TR-75-49

LED X-Y MATRIX DISPLAY

DATA SYSTEMS DIVISION
LITTON SYSTEMS, INCORPORATED

MAY 1975

TECHNICAL REPORT AFFDL-TR-75-49
FINAL REPORT FOR PERIOD 1 APRIL THRU 6 DECEMBER 1974

AIR FORCE FLIGHT DYNAMICS LABORATORY
Air Force Systems Command
Wright-Patterson Air Force Base, Ohio

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number):
The Research and Development Program goal was to fabricate a one-inch by one-inch green LED display surface using flip-chip. It was demonstrated that an LED display of this type can be developed and built for use in the cockpit of advanced military aircraft. Problems experienced with the metallization and isolation in the arrays limited the yield of usable arrays to 24 for a reduced surface area of 1/2-inch by 3/4-inch.

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20. ABSTRACT (Continued)

The display surface has 64 lines per inch capability and is composed of GaP arrays with 8 by 8 LEDs in a 1/8-inch by 1/8-inch flip-chip bondable system. The display surface is annotated by a display generator and display processor to simulate an Attitude Director Indicator for aircraft cockpit displays. A contrast enhancement filter also was developed to increase the contrast ratio to a level that would allow use of the display on a 10,000 foot candle ambient. The filter proved very effective.

The total program conclusively demonstrated that the concept of using an LED high-resolution display for airborne cockpit use is correct.

FOREWARD

This technical report documents the results of an investigation conducted under USAF Contract Number F33615-72-C-1106, Project Number 6190, and Task Number 01. The objective of the investigation was to demonstrate the Light Emitting Diodes (LEDs) can be fabricated into an edge joinable module for use in aircraft instrument displays.

The contract was intiated by the Advanced Display Techniques Group of the Flight Deck Development Branch, Flight Control Division, Air Force Flight Dynamics Laboratory, Wright-Patterson Air Force Base, Ohio. The work was performed under the guidance of Capt. Wayne R. Clements (AFFDL/FGR), Program Manager.

The report covers work conducted during the period of 1 April 1972 through 1 December 1974 and was submitted by the authors on 1 December 1974.

The program at Litton Data Systems Division, 8000 Woodley Avenue, Van Nuys, California, was conducted by the Advanced System Development Department under the supervision of Dr. G. R. Kaelin and A. L. Riggs. Major contributors in the research, development and fabrication of this LED display were R. H. Nakahara, D. M. Piatt, J. G. Price and H. T. Groves.

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SUMMARY

The object of the research and development program for which this final report has been prepared was to develop a one-inch-square, 64-lines-per-inch, green LED monolith display that would be capable of four-edge joining for unlimited growth to any required size. The display was also required to achieve sufficient light output so that at 10,000 fc ambient it could be used in an aircraft cockpit. The development of a contrast enhancement filter was required as part of the program.

The primary objectives were met in the respect that a display surface was developed that meets the requirements of the program, but the display surface was reduced to 1/2 inch by 3/4 inch because the arrays required for the full one-inch-square display could not be obtained. A contrast enhancement filter was developed that allows the display to be viewed in a 10,000 fc ambient. A display generator was developed that is capable of writing alphanumerics and vectors on the display. A display processor was developed to simulate roll and pitch in an aircraft such that a dynamic Attitude Director Indicator (ADI) could be produced on the display. The display exhibits a three point grey scale.

Development of the monolithic flip chip arrays was a partial success. Excellent optical isolation was achieved but problems were encountered in the metallization and electronic isolation. Many shorts developed between the row and column metallization and each short produced a half "on" set of LEDs when the display was operated. Opens developed in the column metallization and produced many "out" columns of LEDs. Diffusion isolation of the columns was a success as was the number of good LEDs in a chip.

Development of the drive system was a total success: all LEDs on the display can be addressed and scanned by the hybrid drive system mounted on the module. Development of the display generator was also totally successful in that alphanumerics and vectors can be selected and placed at any point in the display surface.

The display processor was developed to simulate aircraft movement in the ADI mode. All vectors and alphanumerics can be moved in a simulated roll and pitch motion by use of a small "joystick." The artificial "Horizon" and "Sky" are also moved with the "joystick" control.

A combined circular polarizer, spectrum bandpass, and anti-reflectant front surface filter was developed to provide contrast enhancement. The filter did not meet the goal of 5 to 1 contrast ratio at 10,000 fc but demonstrated a viable approach to the problem of display viewing in an ambient that ranges from 0.01 fc to 10,000 fc. Degradation experienced with the anti-reflectant coating on the filter can be corrected by using a standard coating available from Polaroid or OCL.

This research and development program demonstrated the feasibility of using LEDs for display in advanced military aircraft cockpits. The problem of the shorts and opens in the arrays can be solved by better metallization or a different approach to gain four-edge-stackable arrays.

Advances in efficiency of LEDs in the past two years have now made an LED cockpit display a very viable one, one that can be developed in the present time frame.

SECTION 1

PROGRAM BACKGROUND AND OBJECTIVES

About ten years ago, the Air Force Flight Dynamics Laboratory (AFFDL) of the Air Force Systems Command recognized the serious limitations of Cathode-Ray-Tube (CRT) display devices for applications in military aircraft cockpits and also was aware of rapid advances being made in flat-panel display technology. The need for reliable replacements for the CRT display devices can be appreciated when one considers such factors as reliability, maintainability, and logistic costs that contribute directly to mission success and to the total Cost of Ownership. The need can further be seen in an examination of some of the end-item equipment parameters. For example, CRT displays have a back-to-front depth that is at least as long as the diagonal dimension of the viewing face; thus, to use CRT displays in aircraft cockpits imposes severe limitations on display areas, location, and flexibility. High-voltage power supplies required in CRT display systems introduce safety hazards and limit the achievable system reliability. Perhaps most importantly, modern fighter aircraft are introducing requirements for avionics suites of steadily increasing complexity and sophistication. While the electronics associated with the CRT display benefits to a degree from the same sophistication as the remainder of the avionics suite, the dimensions of the CRT remain large and relatively stable. What is needed is a compact display system that overcomes the inherent limitations of CRT display systems without adding others. Within this decade the major portion of aircraft data handling and processing systems will be completely digital to sense and process all data in preparation for its display to the pilot.

Recognizing the potential of monolithic Light-Emitting-Diode (LED) display systems to overcome the limitations of CRT systems, AFFDL began a development program that can result, in this decade, in a revolutionary advancement in displays for cockpit applications. Specifically, the AFFDL sought the development and fabrication of a prototype flat-panel X-Y Green LED Matrix Module Display System to demonstrate the feasibility of monolithic LED array production, electronics integration, display system utility, and expandability.

In selecting a program contractor, AFFDL acknowledged that the development program to satisfy the Air Force display requirement could not be limited to a simple application of LED technology; instead, the task had to be approached as a total display

system in recognition that it is but a step toward the eventual production of integrated solid-state displays for airborne and other environmentally critical military and space applications. The Air Force selected the Data Systems Division (DSD) of Litton Systems, Inc. to design, fabricate, and test the prototype display, recognizing the DSD abilities to satisfy military system requirements as well as to take maximum advantage of LED technology. For the capability to grow high quality epitaxial gallium phosphide and reproducibly provide arrays of green emitting LEDs, the Division joined forces with the Electronics Products Division of Monsanto Company, recognized as a leader in III-V materials and LED fabrication.

This final report describes the prototype LED X-Y Matrix Display produced and tested under Contract F33615-72-C-1106 in the period from April 1972 to July 1974. The selected technical approach called for the Zn diffusion of light emitting junctions in vapor phase epitaxially grown gallium phosphide to produce monolithic 8-diode by 8-diode arrays measuring only 0.125 inch in each of the two planar dimensions. Eight of these arrays (in a 2 by 4 arrangement and metallized in an X-Y pattern) are bonded, emitting junction down to a multilayer metallized ceramic substrate 1/4 inch by 1/2 inch in area to form an element called a stack. Each stack is packaged with integral addressing and scanning circuitry enabling a parallel Y and serial X mode of operation. The stack so produced is complemented by an MOS shift register that is mounted on a mother-board and serves as the display refresh memory for each stack. The board also contains the display generator for line and character generation with random positioning.

A 1-inch by 1-inch display requires eight stacks, but the low yield experienced in producing the diode arrays limited the prototype model display area to 1/2 inch by 3/4 inch. This area proved to be large enough to permit full evaluation of system capabilities to the point that the technical feasibility of the display concept is considered fully established. The prototype model was delivered to AFFDL on 13 September 1974.

SECTION 2

DESCRIPTION OF LED DISPLAY EQUIPMENT

2.1 INTRODUCTION

The X-Y LED equipment consists of the following subassemblies:

a. LED Display Surface.

b. LED Drive Circuits.

c. Display Generator.

d. Display Processor.

e. Contrast Enhancement Filter.

f. X-Y Control Stick.

The units are packaged into three mechanical subassemblies as shown in Figure 1. The LED display surface, drive circuits, and contrast enhancement filter are contained in the display head unit. The display generator, display programmer, controls, and power supplies are contained in the main unit and the control stick is in a separate unit.

The purpose of this development was to demonstrate the feasibility of using an X-Y addressable Green LED display as a multimode instrument in advanced military airborne cockpits. The display is composed of monolithic arrays of green GaP LEDs that are metallized in X and Y on one side only such that they can be flip-chip bonded. The requirements imposed on the arrays, LED scanning, and display-surface filter were as follows:

a. Center-to-center diode spacing will be approximately 16 mils. The diode size of 8 mils diameter is desired but deviations for construction or efficiency reasons will be considered.

b. The average brightness of an 8 mil diode in the 10K ft-L ambient operational mode after filtering should be 80 to 100 ft-L with a background brightness of 40 to 50 ft-L resulting from the reflected ambient and leakage in off diodes. Uniformity should be held to ±10 percent of operating brightness.

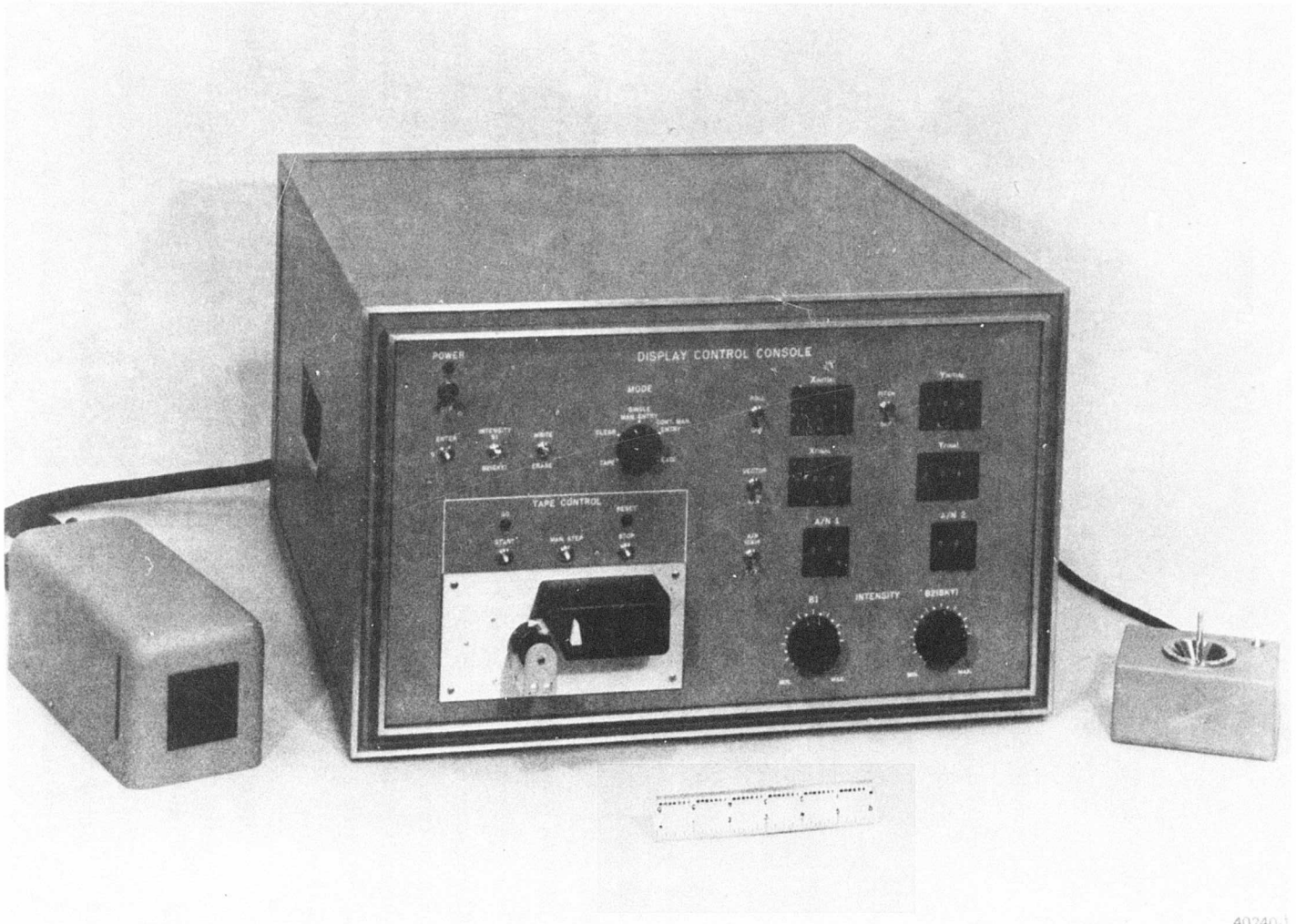

Figure 1. X-Y LED matrix module.

c. The contrast filter should be a combined circular polarized, anti-glare coated, narrow bandpass filter which makes the display face appear as a solid piece when illuminated with 10K ft-L. The diodes or the electrode patterns are not to be distinguished from the background.

d. All connections to the diodes will ultimately be brought to the rear so that the modules will be connected together only through the rear pins.

e. The display should be dimmable to 0.05 ft-L with variations of ±10 percent of operational brightness being used.

f. A scanning technique is required in which power is applied to the LEDs in a dot at a time or row at a time in an X-Y drive technique. To prevent eye motion flicker, a refresh rate of 1 kHz is required. A refresh memory in the module or the mother board is considered necessary to reduce EMI.

g. The center-to-center diode spacing between edge diodes when two modules are placed side by side should be equivalent to internal diode spacing, or approximately 16 mils.

h. The heat generated by 20 percent of the diodes being used must be dissipated using only forced ambient air cooling at the rear of the display.

All requirements listed above were met with the exception of the brightness through the filter and desired contrast. This brightness was measured at 43.5 ft-L as compared to the desired 80 to 100 ft-L. Increases in LED efficiency have now been made that will permit attainment of the 80 to 100 ft-L brightness through the filter.

The subassemblies enumerated above are described individually in this section. An operator's manual, presented as Appendix A of this report, provides additional description within the context of equipment operation.

2.2 LED ARRAY FABRICATION

The basic configuration of an array, prior to metallization, is shown schematically in Figure 2. This array consists of 0.008-inch-diameter LEDs placed on 0.0156-inch centers in both the X and Y directions. The common cathode of all the LEDs in a given column (Y-direction) is electrically isolated from all other LED cathodes by stripe p-type isolation diffusions which penetrate the top n-type layer, join

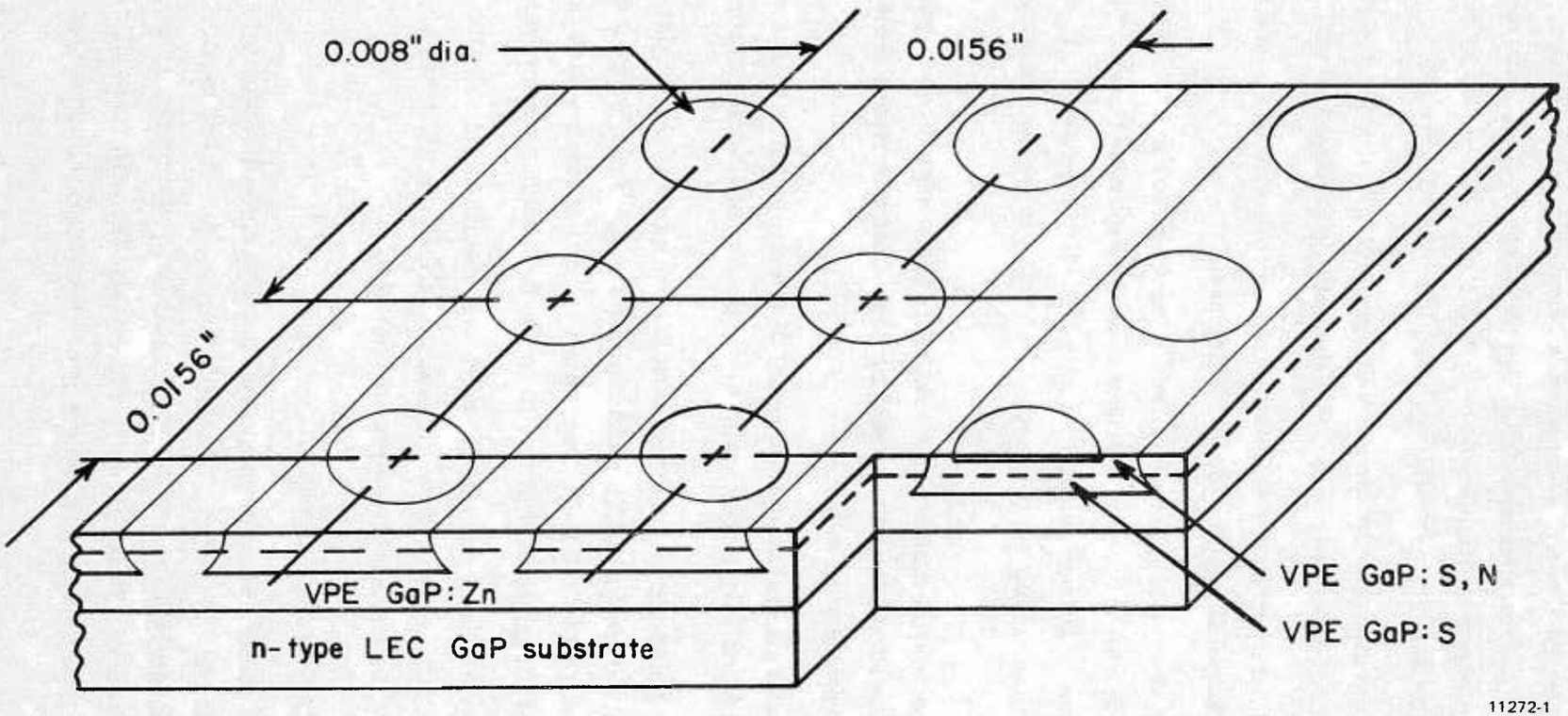

Figure 2. Array configuration prior to metallization.

with the buried p-type layer, and extend over the full length of the chip. Matrix addressability is then achieved by contacting each of the isolated n-type regions forming the column address and by applying metallization stripes in the X-direction which contact various rows of LED anodes thus forming the row address.

The GaP epitaxial wafers used in this work are grown by standard techniques described previously[1] on (100)-oriented GaP LED substrates. In the present case Zn is substituted for the conventional n-type dopants S or Te during the first ≈ 50 μm of epitaxial growth. The remaining ≈ 50 μm of growth is then formed n-type by using the dopants S or Te. The final 25 μm of material to grow is doped with nitrogen as described previously[2,3] to optimize electroluminescent performance.

The carrier concentration in the buried p-type epitaxial layer is nominally 0.7 to 3 x 10^{17} cm^{-3}. The carrier concentration in the n-type epitaxial layer is on the order of 1 x 10^{17} cm^{-3}, but is intentionally profiled so that the concentration in the vicinity of the light emitting junction is less than $10^{17}/cm^3$ while remaining higher elsewhere. This is done to minimize lateral resistance in the isolated n-region while maintaining the proper ($n < 10^{17}/cm^3$) carrier concentration in the vicinity of the active junction consistent with optimum electroluminescent performance.[4]

Nitrogen doping is confined to the vicinity of the LED junctions in order to improve the transparency of the total structure and visibility of the array through the substrate.[4] The radiative recombination generated in nitrogen doped GaP layers results in predominantly A-line emission (λ = 5650Å, $h\gamma$ = 2.194 eV) and associated phonon replicas[3,4] at room temperature which is below the band gap energy

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[1] M. G. Craford, W. O. Groves, A. H. Herzog, and D. E. Hill, "Electroluminescence and Electrical Properties of High-Purity Vapor-Grown GaP," J. Appl. Phys. vol. 42, p. 2751, June 1971.

[2] W. O. Groves, A. H. Herzog, and M. G. Craford, "The Effect of Nitrogen Doping on $GaAs_{1-x}P_x$ Electroluminescent Diodes," Appl. Phys. Lett. vol. 19, p. 184, Sept., 1971, and M. G. Craford, D. L. Keune, W. O. Groves, and A. H. Herzog, "The Luminescent Properties of Nitrogen Doped GaAsP Light Emitting Diodes," J. Electron. Mater., vol. 2, p. 137, Feb., 1973.

[3] M. G. Craford, R. W. Shaw, A. H. Herzog, and W. O. Groves, "Radiative Recombination Mechanisms in GaAsP Diodes with and without Nitrogen Doping," J. Appl. Phys. vol. 43, p. 4075, Oct., 1972.

[4] R. A. Logan, H. G. White, and W. Wiegmann, "Efficient Green Electroluminescent Junctions in GaP," Solid-State Electron., vol. 14, p. 55, Jan., 1971.

(Eg = 2.25 eV) of nitrogen free GaP. For that reason, junction electroluminescence in these structures is visible from either side of the structure, and arrays fabricated from material of this type may be flip-chip bonded and viewed through the substrate. This feature has special significance in that, due to the absence of wire bonds at the edges of the chips, the arrays may be stacked edge-to-edge in both the X and Y directions while maintaining the same LED line spacing across the chip-to-chip interface. This enables the application of these arrays in graphical as well as video displays with various formats.

Columns of electrically isolated n-type material are formed by a closed-ampoule Zn diffusion through a 0.00075-inch wide stripe-pattern Si_3N_4 diffusion mask (see Figure 3). The Si_3N_4 used in the work is deposited using conventional CVD techniques[5] and processed into diffusion masks by standard photoresist methods.[6] A cross-section of the structure after isolation diffusion is shown in Figure 4. Following the isolation diffusion, the wafer surface is recoated with Si_3N_4 and again photoprocessed to open 0.008-inch-diameter diffusion windows on 0.0156-inch centers for the LED anode (see Figure 5). The active emitter junctions are then formed by a closed-ampoule Zn diffusion.

Ohmic contacts are formed on the n-type cathode regions using Au-Ge. N-type contacts are positioned between each pair of LED anodes in a given column (Figure 6) and are interconnected with a sputtered Mo/Au/Mo interconnection metallization (Figure 7), similar to that employed in the fabrication of Si integrated circuits.[7] A layer of sputtered glass is then deposited to serve as insulation between row and column metallization. Vias are then opened in the glass layer exposing the p-type ohmic contacts. A sputtered Mo/Au/Mo interconnection metallization (Figure 8) is then applied which connects the LED anodes in a given row. A final layer of sputtered glass is applied to passivate the structure. Vias in the final layer of glass are opened over portions of the row and column metallization (Figure 9) and are filled with sputtered Au or Ni followed by Au to permit contacting with flip-chip bonds.

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(5) J.T. Milek, Silicon Nitride for Microelectronic Applications, Handbook of Electronic Materials, vol. 3 and vol. 6, Plenum Press (1971).

(6) L.I. Maissel and R. Glang, Handbook of Thin Film Technology, McGraw-Hill (1970).

(7) J.A. Cunningham, "Expanded Contacts and Interconnections to Monolithic Silicon Integrated Circuits, "Solid-State Electron., vol. 8, p. 735, 1965.

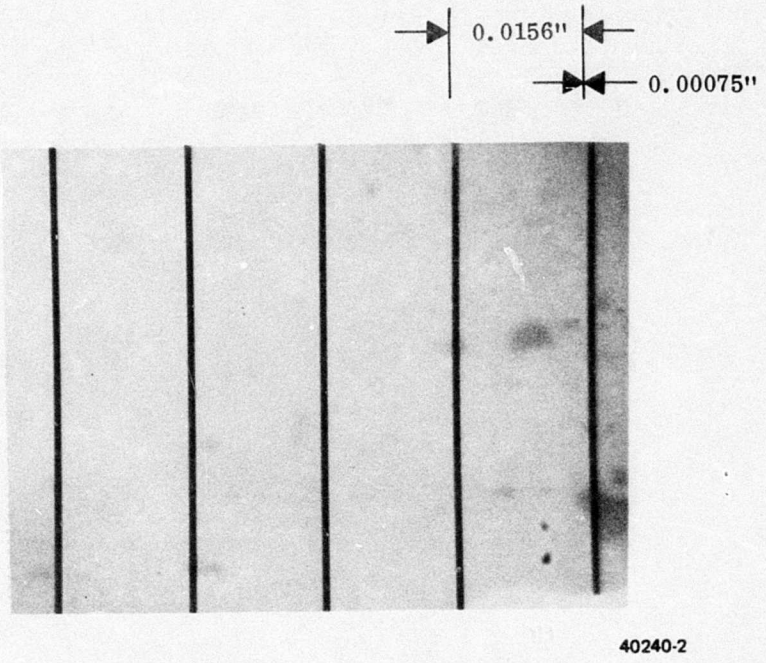

Figure 3. Photograph at 50X of isolation diffusion pattern.

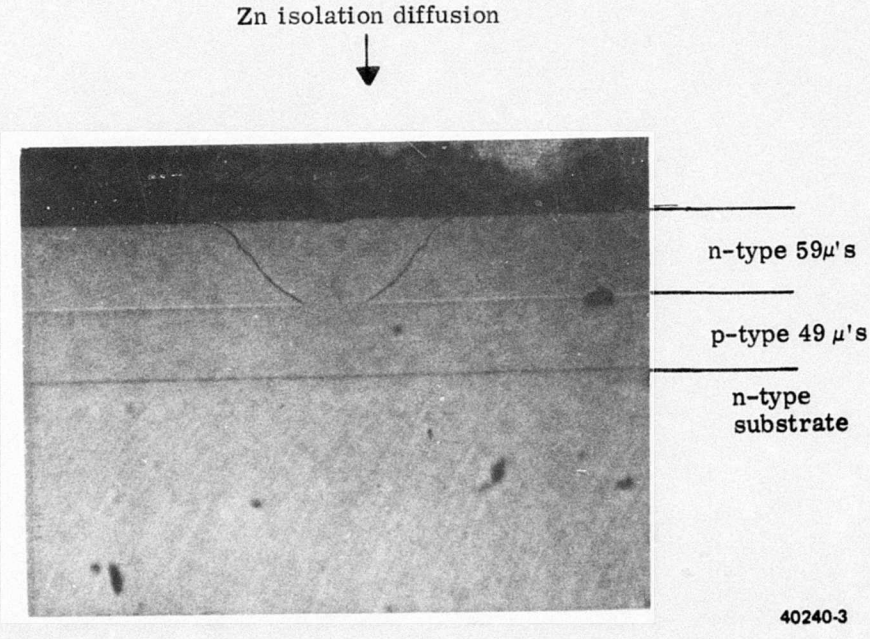

Figure 4. Photomicrograph (200X) of stain-etched cross-section of isolation diffusion.

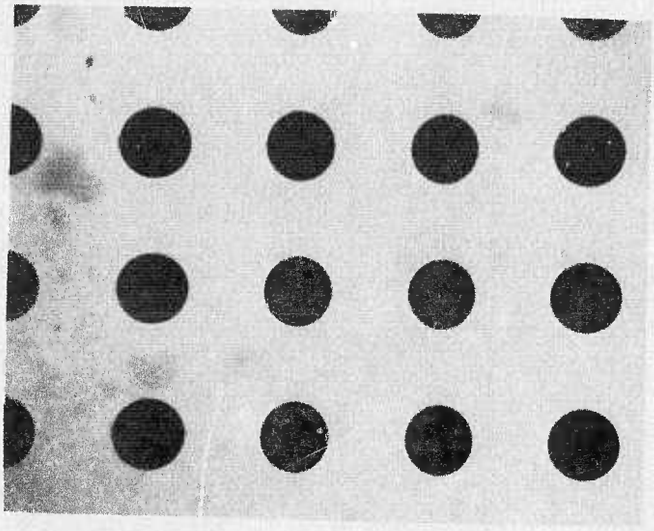

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Figure 5. Photograph of LED diffusion pattern at 50X.

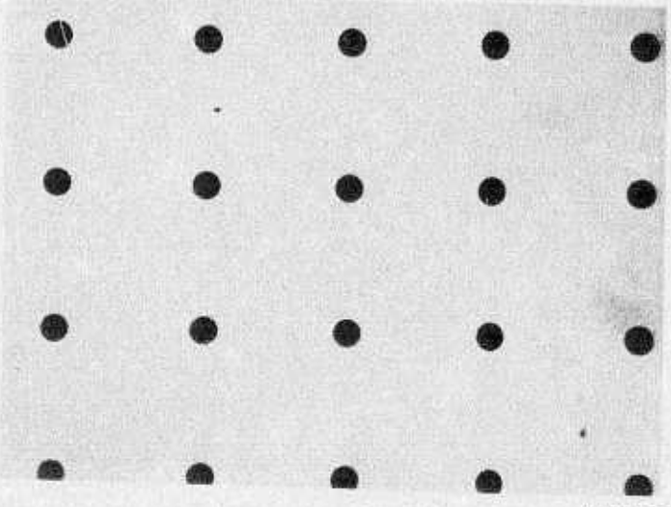

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Figure 6. Photograph of n-type ohmic contact pattern at 50X.

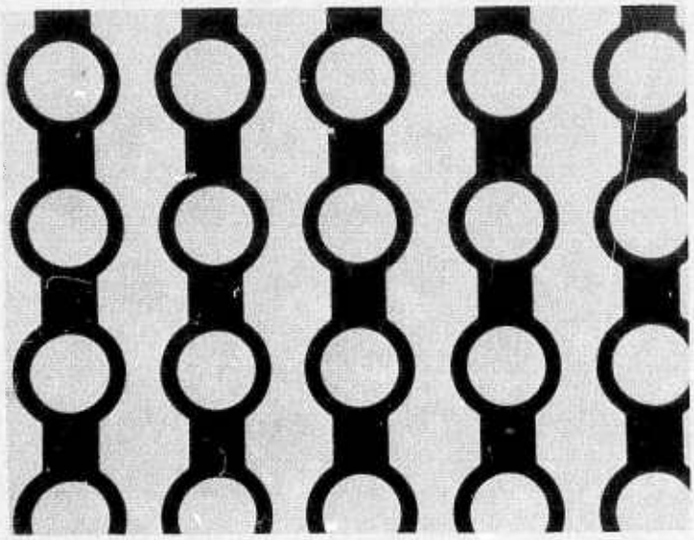


Figure 7. Photograph of n-interconnect pattern at 50X.

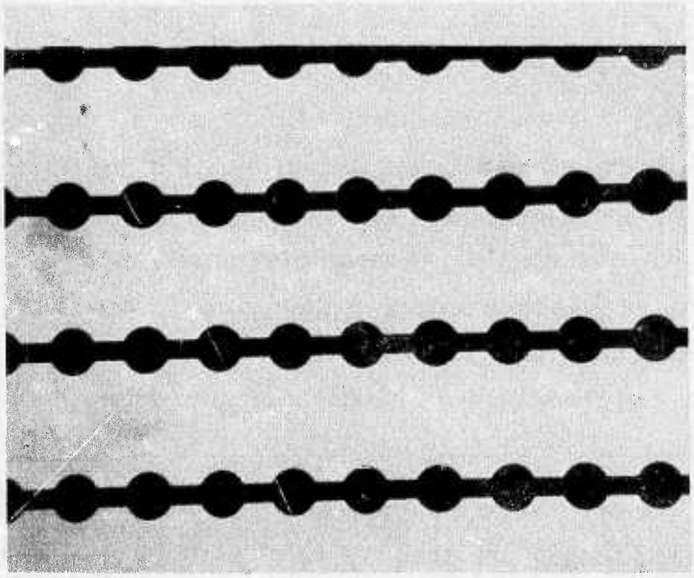
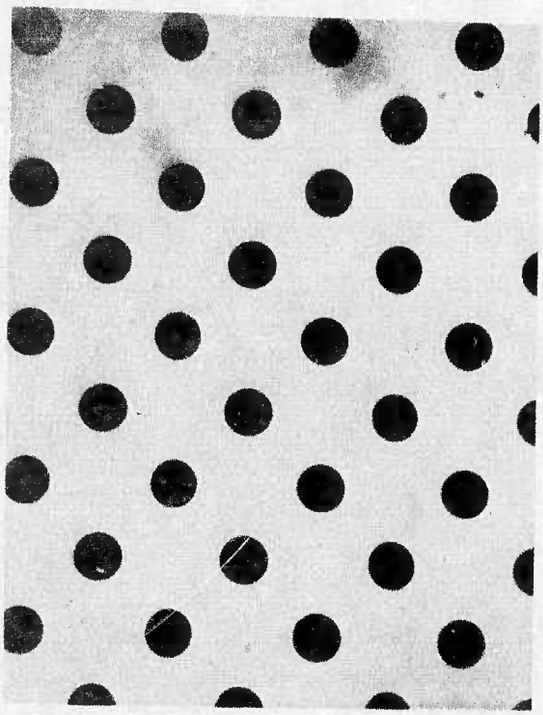


Figure 8. Photograph of p-interconnect pattern at 50X.



40240-8

Figure 9. Photograph of flip-chip bonding pad pattern at 50X.

Wafers are lapped and polished on the substrate side to a final thickness of $\approx 150\,\mu$m to minimize absorption in the substrate and scattering at the inactive surface. This is particularly important where the array is to be viewed through the substrate. Wafers are then separated into 8 x 8 element array chips with a diamond blade dicing saw.

2.3 ASSEMBLY OF LED CHIPS INTO DISPLAY SURFACE

The 1/8-inch by 1/8-inch monolithic LED chips are assembled into 1/2-inch by 1/2-inch arrays on a ceramic substrate. Solder bumps in the pattern shown in Figure 10 are developed on the metallized side of each array near the outer edge. Each X and Y line has a bump on each end to make contact with the alumina substrate; only one of the two bumps is needed to ensure contact for the eight LEDs in that particular X or Y strip and the second bump is used for redundancy. Each monolithic array has 32 solder bumps around the edge and four in the center, where the four in the center are for support only.

The monolithic arrays are then mounted on a multilayer ceramic substrate (Figure 11) that is 1/2-inch by 1/2-inch and receives 16 of the arrays for a total of 1024 LEDs (32 x 32). The arrays are reflow soldered to the substrate in a single heat.

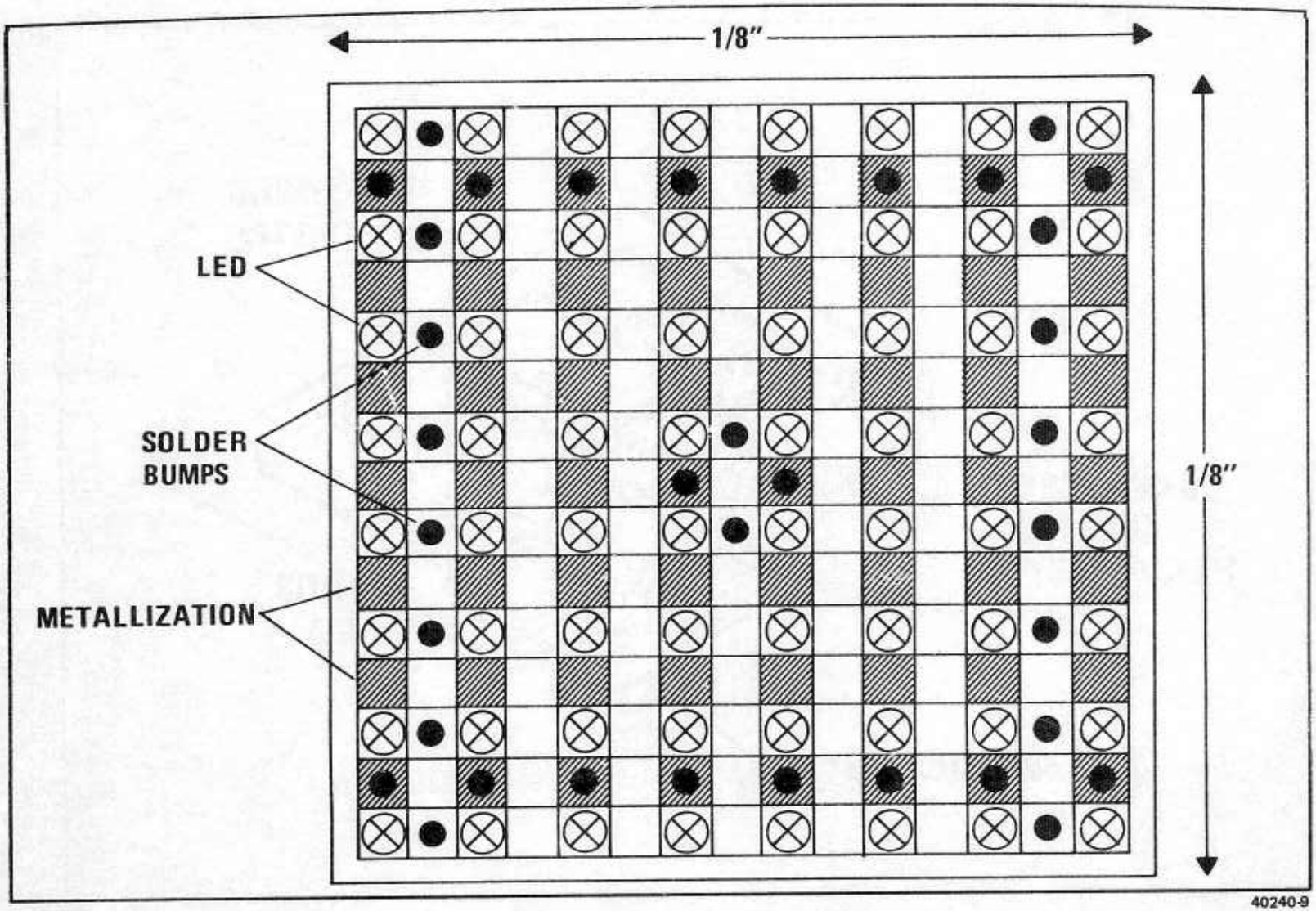


Figure 10. Solder bump for monolithic array.

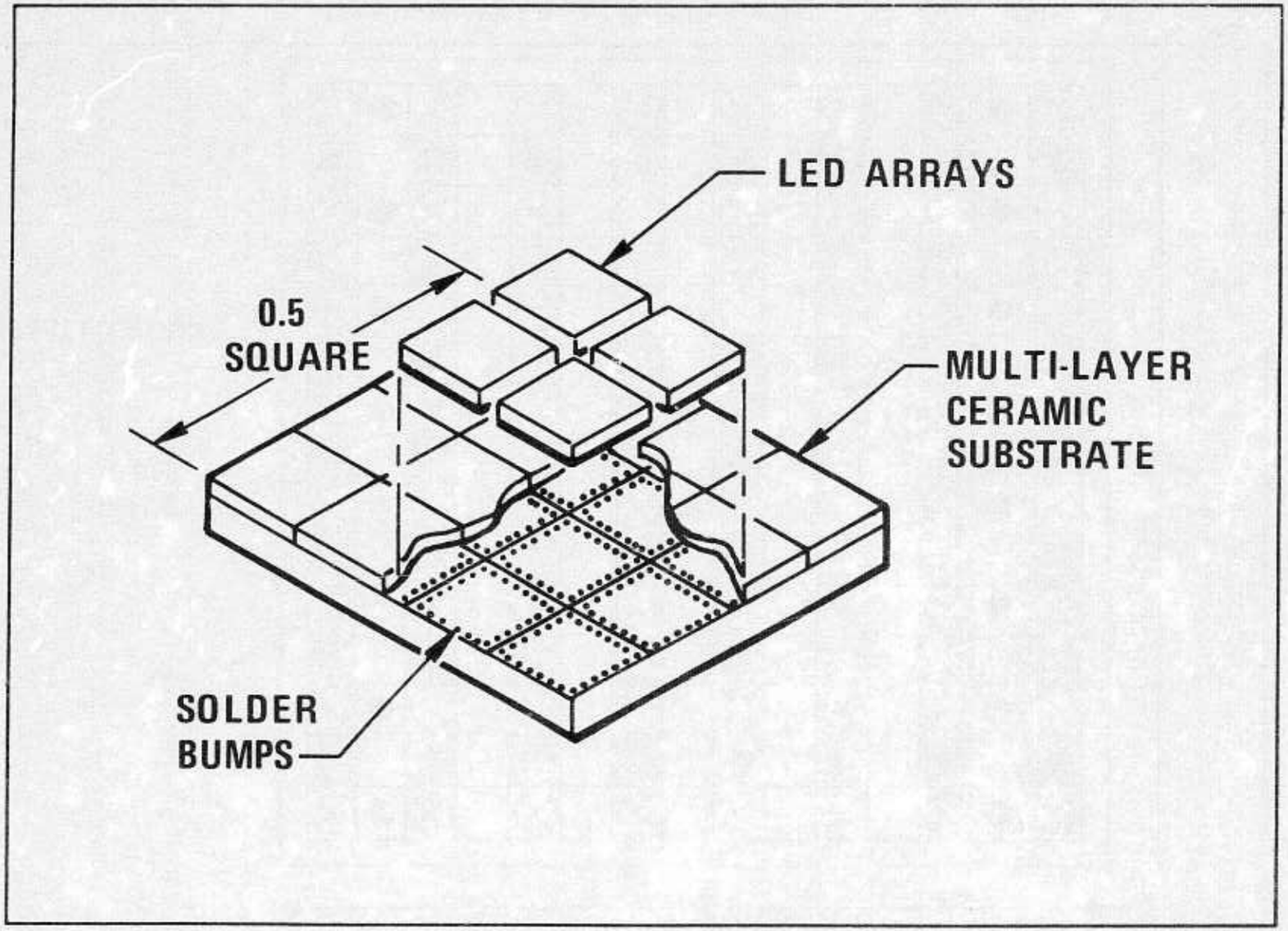


Figure 11. LED arrays mounted on multilayer ceramic.

Alignment of the arrays is accomplished by the surface tension of the solder bumps on the array and on the substrate. The ceramic substrate extends the 8 x 8 X-Y pattern of the arrays to a 16 x 64 X-Y pattern that is terminated in an 80-pin connector to interface with the drive circuits. As explained in 2.4, the LEDs are scanned in a column-of-64 by row-of-16 pattern even though the physical grouping is 32 x 32 LEDs.

Four of the 1/2-inch by 1/2-inch substrates with the mounted arrays can be mechanically mounted to form a 1-inch by 1-inch display containing 4096 LEDs in a 64 x 64 matrix. Each 1/2-inch by 1/2-inch substrate is a "stand alone" display refreshed at approximately 1000 Hz. The 1-inch by 1-inch modules could be edge-joined to form a display of any size desired without interruption of the total display surface.

After the 1/2-inch by 1/2-inch substrates have been edge-joined, a contrast enhancement filter is placed over the viewing side of the array to increase the contrast of the display in a high ambient. The contrast filter is optically coupled to the LEDs by using an optical matching gel to reduce the internal reflectants of the display.

2.4 CONTRAST ENHANCING FILTER

The filter shown in Figure 2-12 and described in this subsection was developed to enhance the contrast of the LED display surface to a point that permits reading it in a 10,000 ft-L cockpit ambient. Detailed information presented here describes the filter development chronologically.

2.4.1 Filter Design Approach

A theoretically ideal contrast enhancing filter would be totally anisotropic, absorbing all light radiation falling on one surface while transmitting all display-originated light in the opposite direction. With such a filter, any self-luminous display element would be bright against a black background. A realizable filter, however, can have only limited anisotropy and must be designed around the performance and use parameters of a specific display. It is possible then to establish filters that approximate anisotropy for the particular conditions involved. Mechanical louvers are not suitable for this application because they give relatively small attenuation of incident light through the viewing angle needed to read the display. Polarization elements can be used, providing less attenuation of nonpolarized emitted light while absorbing cross-polarized light. Circular polarization is particularly effective since the incident light transmitted by the filter will, on specular reflection from the display,

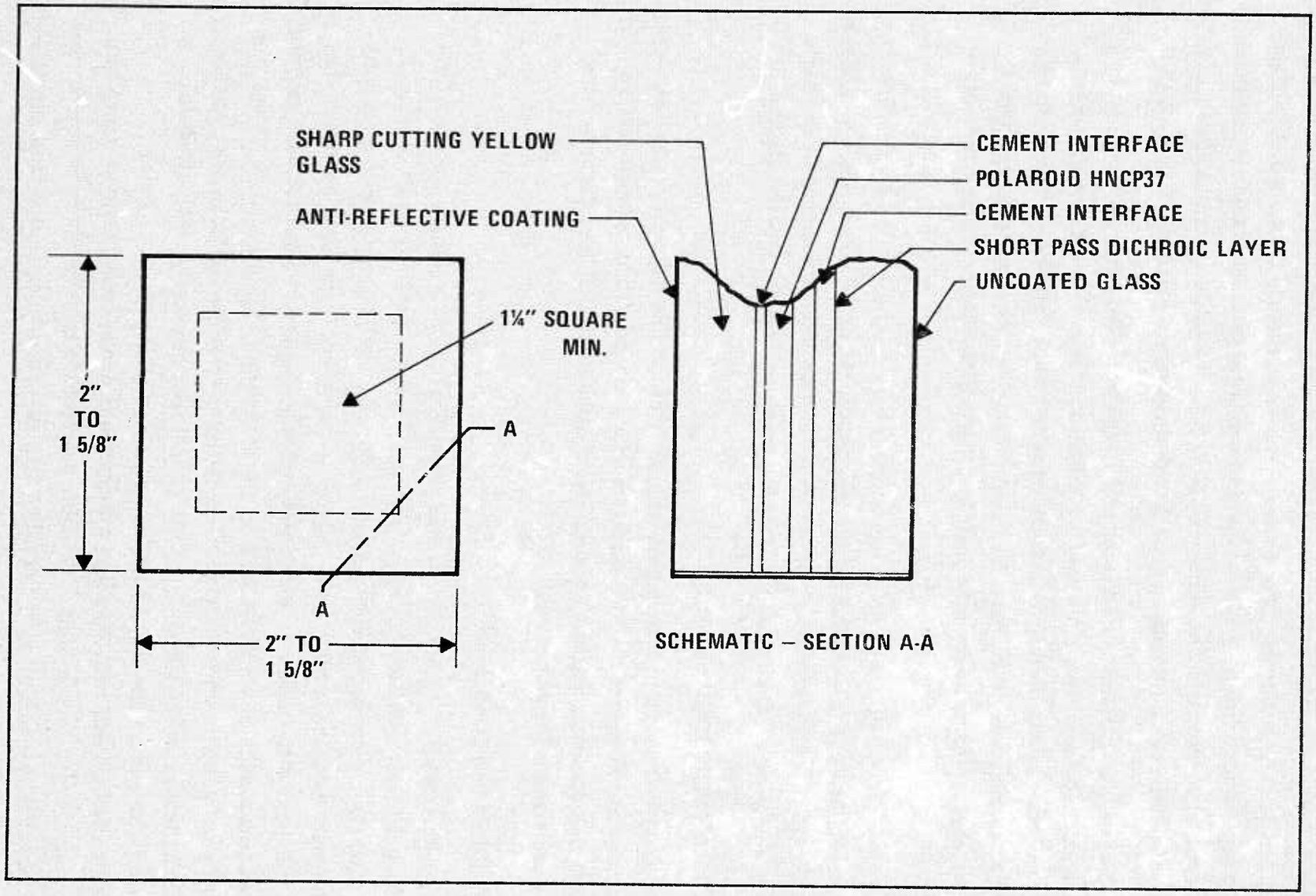


Figure 12. Contrast enhancing filter.

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then be absorbed. Bandpass filters, which absorb all spectral bands except that containing the display emission, have some anisotropy but the filter transmits, with the same minimal attenuation, all incident light contained in the bandpass. The reflectivity from the surfaces of the filter can be reduced by using antireflection coatings and by careful selection of materials. Thus, a combination of bandpass and circular polarization, together with anti-reflection treatment, provides the most suitable filter for this application.

For the prototype EADI display, using the developmental monolithic GaP LED arrays, the filter design was based on a worst-case ambient illumination level of 10,000 ft-L and a target efficiency for the LEDs. The efficiency of the diodes in production was expected to be such that the average diode brightness would be 200 ft-L, driven by the 40 ma, 5.5 percent duty cycle pulse generated for the display. (The diode brightness is defined for this application as the brightness through the GaP array, measured perpendicular to the array surface.) The diodes in the arrays actually received and used in the prototype display had an average brightness of approximately 90 ft-L as driven in the display.

Other factors considered significant in the filter designs included the spectral distributions of the ambient illumination and of the diode emission, the reflectivity of the GaP array, the geometrical distribution of ambient light, and any polarization parameters. Since the display legibility criteria would necessarily depend on eye response, the spectral distributions must be considered in terms of visual effect, rather than energy. For example, the sea level daylight ambient has close to equal energy in the spectral bands from 525 to 575 nm and 650 to 700 nm, but the energy in the latter contributes less than two percent to the total visual effect of the daylight, while the first band contributes about 43 percent. The emission of the GaP diodes is essentially monochromatic, centered around 557 nm, with a bandwidth of approximately 20 nm. Since this is entirely within the band of sunlight producing the maximum visual effect, simple bandpass filtering to enhance the display is precluded. The high reflectivity of the GaP surface implies that even with a perfectly matched bandpass filter, extremely high levels of ambient light will be transmitted through the filter to illuminate the surface of the display and then be reflected back to the observer in exactly the same spectral band as the diode emission, effectively masking the light from the diodes.

The emitting junctions of the diodes in the monolithic GaP arrays are formed close to the surface of the crystal wafer. The contact metallization, through which

each array is bonded to module substrate, is formed on this surface. The diode emission, then, is seen through the wafer. This does provide for complete visibility of the emitting junction, with no obscuration by contact metallization, but it also introduces several factors which are not necessarily advantageous.

The GaP crystal is transparent to the emission from the junction and the base surface is well polished, minimizing any diffusion of the light from each diode. However, the index of refraction for the GaP crystal is very high: approximately 3.5 for $\lambda = 557$, the wave length of the emitted light. This introduces two factors tending to attenuate the light from the junction. Fresnel reflectivity at the interface with air is approximately 31 percent, representing an effective loss of light. Also, the angle of total internal reflection at this surface is approximately 16.5 degrees. Hence, although the junction may be considered as a virtual Lambertian emitter, only the light emitted through a relatively small solid angle (approximately 0.09 steradian) actually leaves the crystal at an air interface. The high Fresnel reflectivity also applies to the reflectivity of ambient light. The specular reflection of light from the surface of the GaP crystal is up to 35 percent of the reflectivity from a good first surface mirror. This high reflectivity eliminates the usefulness of either simple bandpass filters or louver type contrast enhancement techniques. However, since this is virtually all Fresnel reflection, the reflected light does show complete vector rotation and makes the use of a circular polarizing filter particularly effective.

The other important reflectivity factor to be considered for any filter array is the ambient light reflected from the surfaces of the filter array. Consider, as the worst case condition, an aircraft cockpit with illumination levels on the display face of 10,000 fc provided by sunlight reflected from a cloud layer and brilliantly and diffusedly lighting up the entire display. Under this condition, the total reflectivity from the filter cannot be allowed to exceed one percent, which would produce an apparent brightness of 100 ft-L at any point on the display face. As an actual design target, the reflectivity of the filter was set for 0.5 percent. This implies applying an antireflection coating producing less than 0.3 percent reflectivity (as measured in luminosity or eye response units). Additional reflectivity will result from every interface in the filter-display assembly which will have a residual reflectivity of 0.1 to 0.2 percent, even though all media are selected and matched to minimize reflectivities. The primary interface to be considered is the interface between the glass carrying the antireflection coating and the circular polarizing lamination. Since all surfaces are highly polished, most residual reflections from surfaces behind the circular

polarizer are absorbed by it. The difference in index of refraction between the glass and the circular polarizing material is small, and the cement can be selected to further minimize any residual reflections.

Graphical and numerical calculations of the reflectivity and transmissivities of the potential filter materials in various combinations preceded experimental verification of the practicality of the contrast enhancement filters. It was easily demonstrated that no bandpass filter could be constructed that would produce significant contrast enhancements. The most efficient combination which could be formulated, transmitting approximately 85 percent of the LED emitted light, also permitted over 3500 fc illumination on the substrate, in precisely the same wave band providing somewhat over 1000 fL surface brightness. The 200 fL target diode brightness becomes almost imperceptible against this background. Brief tests with plastic and glass filter components verified the calculations, showing that although there was a slight increase in the visibility of an activated diode at moderate ambient light levels (up to 1500 fc), the diode could not be seen to be lit under high light levels.

Similarly, tests with "Hycon" and 3-M Corporation's "Light Control Films," two different designs of louvered contrast enhancement materials, showed improved visibility in moderate light levels. Here, however, there was also great dependence on the angle between the source of illumination and the face of the display. There was not sufficient improvement in contrast to permit recognition of whether the test diode was activated at high light levels.

On the other hand, calculations showed that with a filter incorporating a circular polarizer, the primary veiling light would be light reflected from the filter itself rather than light reflected from the display surface. It was evident that even though the best circular polarizer would attenuate the light from the diodes, transmitting only 37 percent of its emission, the brightness of surface surrounding the active diode would be decreased to levels permitting good contrast even in the 10,000 ft-L ambient.

The effectiveness of the circular polarizer is wavelength dependent. The quarter wave retardation film laminated to the neutral linear polarizer produces completely circular polarized light only for light of wavelengths close to 500 nm. This circularly polarized light is very efficiently reversed in phase by reflection from the GaP substrate and then absorbed by the polarizer. As the wavelength of the light departs from the wavelength for which the quarter wave retardation layer is designed, the reflectivity increases. That is, light from the blue and red portions of the spectrum is not as

completely absorbed. However, the peak effectiveness of the circular polarizer coincides with the emission of the GaP diode. Hence, the regions of the spectrum not thoroughly blocked by the circular polarizer can be absorbed by a bandpass filter with high transmission for the diode emission. Tests made with samples of bandpass and circularly polarizing materials verified this fact and attention was concentrated on obtaining the most efficient antireflection coating available. Tests indicated that multilayer and reflection coatings could be formulated exceeding the performance of most published curves. Sample coatings were obtained that showed less than 0.2 percent reflectivity, as measured in visual units. (It should be noted that for this application, increased reflectivity in extremes of the visible spectrum, if required to achieve reduced reflectivity near the 550 nm region, does not significantly increase the perceptible brightness of the surface.) Assembling these sample coatings with the circular polarizer and bandpass elements produced a filter that permitted excellent visibility of an illuminated GaP diode in the direct light of a "sun gun" providing 10,000 ft-L illumination on the face of the filter. On the basis of these tests and calculation, a procurement specification was generated, and prototype filters were ordered from the Herron Optical Company, Division of Bausch and Lomb.

2.4.2 Filter Gel Interface

In the course of the filter development, attention was given to the possibility of minimizing Fresnel losses at the surface of the GaP crystal by introducing a high index medium between the GaP surface and the filter. The optimum medium, with index of refraction of about 2.0, would reduce the total loss to about 9 percent, considering reflectivity at both the interfaces between the medium and GaP and filter, respectively, as compared to the 31 percent loss at an air-GaP interface. The most practical materials to be used, however, are silicone or urethane polymers, which could be formulated to form a soft gel layer on the filter which could "wet" (i.e., form optical contact with) the GaP crystal surface without damaging or permanently adhering to it. The materials available to meet these criteria have indices ranging from 1.45 to 1.64. The net Fresnel losses with these materials are approximately 14 percent. (The possibility of using such an interface led to specifying that the last surface of the filter assembly be uncoated glass.)

2.4.3 Filter Tests

Filters initially received from Herron Optical Company used Corning 3-68 filter glass as the first element of the assembly, on which the multilayer antireflection

coating (a modified MARC-IV coating) was deposited. The filter appeared to be satisfactory on initial inspection and provided good contrast enhancement. However, there was a rapid deterioration of this first element, showing itself as a diffuse overveiling of light when the surface was illuminated. (It was not established whether this was a selective scattering or a fluorescence phenomenon but there appeared to be some shift in the spectral distribution of the light from the element as compared to the incident light.) This light completely masked the display under even moderate light levels. This filter was also assembled with an incorrect short-pass dichroic layer.

The filters were reassembled, after some difficulty with cementing, using Hoya 0-54 glass for the first element. These filters appeared to meet the specifications and one of this second lot was assembled to the display.

Another filter of this lot was also tested for polarization effects. One of the filters of the second lot was tested by ECOM, and it was found that the residual reflectivity varied as a function of rotation around an axis perpendicular to the filter. These measurements could be reproduced in our laboratory, but only with a diffuse reflector mounted behind the filter. With an array of GaP wafers behind the filter, the differences became negligible. A polarization analyzer on the photometer showed that the residual reflections from the filter contained linearly polarized components. This tends to indicate that the differences in reflectivity measured as a function of filter rotation resulted from interaction between the linear, polarizing component of the filter assembly and the depolarizing effects of a diffusing surface behind the filter. Since the GaP array does not depolarize the light, an equivalent effect is not perceived when the filter is measured against a GaP array or other specular reflecting surface.

2.4.4 Filter Performance

One filter of the second lot was mounted with the prototype display head, and its contrast enhancing performance evaluated with and without the gel interface and compared to a high efficiency and reflection coated neutral polarizer. Measurements were made with normal drive circuit parameters. Data was recorded for a single diode within the aircraft symbol on the EADI selected as representative of satisfactorily functioning elements by comparison with other functioning elements on the display. (The brightest diode of the array was approximately 1-1/2 times as bright.) Brightness measurements were made under several conditions of varying display density and "sky" brightness. Ambient lighting conditions included typical laboratory ambient (approximately 60 fc as measured on the display surface) and with high

level illumination (approximately 8.2K fc on the face of the display) provided by a quartz-iodine flood lamp filtered to simulate sunlight. Measurements were made with a Gamma Photometer, the probe of which subtends an area approximately three times the emitting area of the diode.

It is virtually impossible to see the illuminated diodes under the high ambient brightness without a contrast enhancing filter. The EADI patterns are readily legible under the same lighting conditions with any of the three filters used in these measurements. Subjectively, the best contrasts appeared to result from the HEA coated HCNP37 or the gel interfaced filter. (Under the high illumination levels, the face of the special filter (C.E. Filter #2) appears to be a little foggy.)

The effect of the gel interface was particularly noticeable, producing approximately a 25 percent increase in apparent diode brightness under given operating conditions.

2.5 LED DRIVE CIRCUITS

Each 1-inch by 1/2-inch LED substrate is scanned at a variable rate with a 5.9 percent duty cycle for each LED. The substrate is functionally organized as shown in Figure 13 into 16 columns by 64 rows. On-off data is loaded into the 64 row driver through four ports simultaneously. After all rows are loaded, the column associated with this information is turned on to display the data. Each of the 16 columns is scanned in this manner and each column sink must be capable of sinking 64 by 40 ma or 2.56 amperes. Each row driver must be capable of supplying a current of 40 ma to one LED at a time.

A row driver is composed of two separate drivers, one for the normal or bright data and one for the "Sky" or dim data. The row driver (see Figure 14) is a constant current source which operates the LEDs with a constant 40-ma pulse regardless of the voltage drop in the LED and the current sink. Eight of the constant current sinks are packaged in a hybrid package with an 8-bit shift register for the bright data and an 8-bit shift register for the dim data. Eight of these packages are used to drive a 1/2-inch by 1/2-inch substrate of 1024 LEDs in a 64 by 16 matrix.

The column sink must be capable of sinking current for 64 LEDs at 40 ma each or 2.56 amps. The sink is composed of four transistors in parallel for the current capability with a Darlington driver. Sixteen of the current sinks are packaged in a hybrid substrate with four 4-bit shift registers for a package capability of 16 bits. The power dissipation in the package is for one sink at a time on and therefore, not excessive. The current sink (Figure 15) has been labeled MC1044 and one is used per 1/2-inch by 1/2-inch substrate. Each MC1044 is packaged with eight MC1045's to form a display head driver card as illustrated in Figure 16.

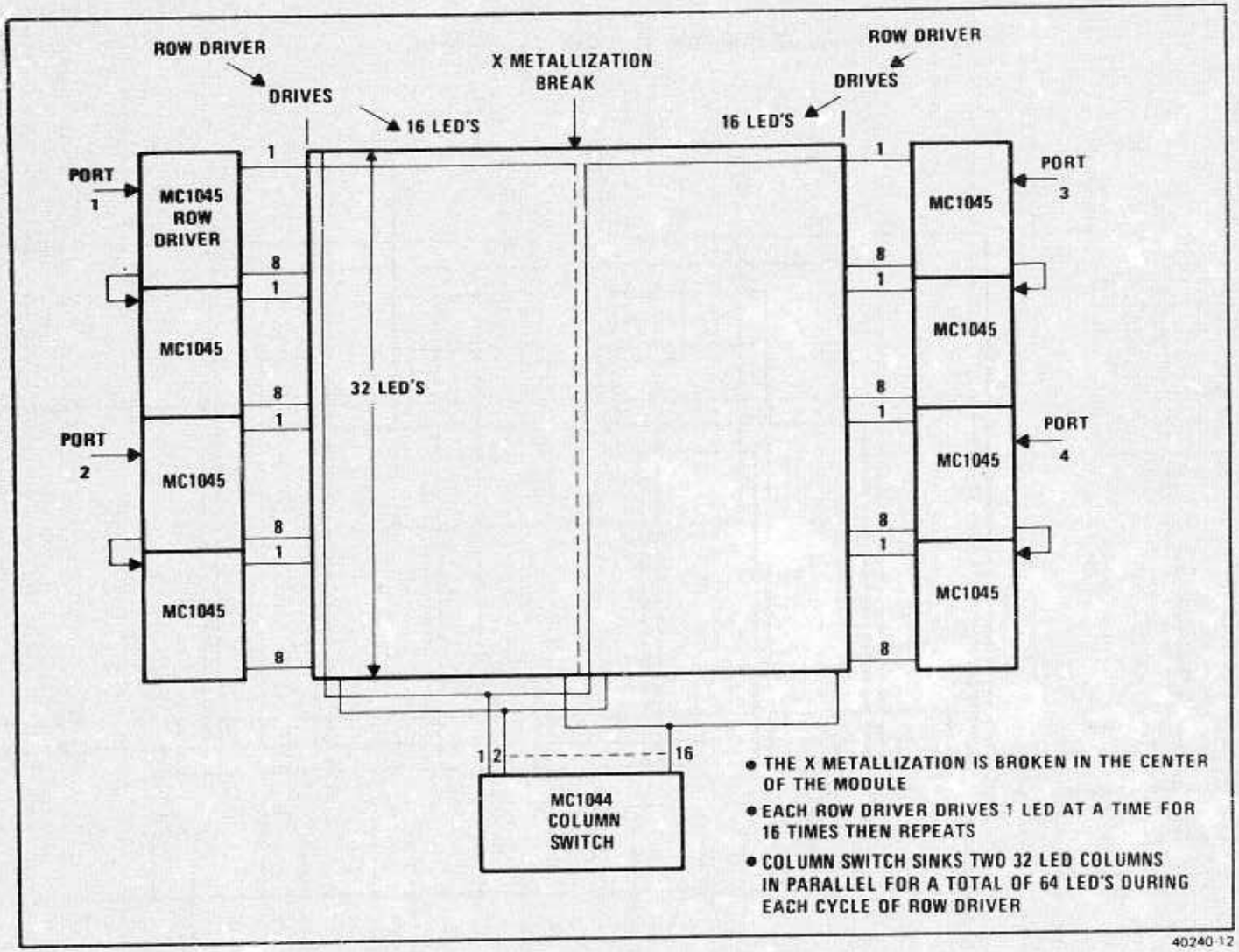
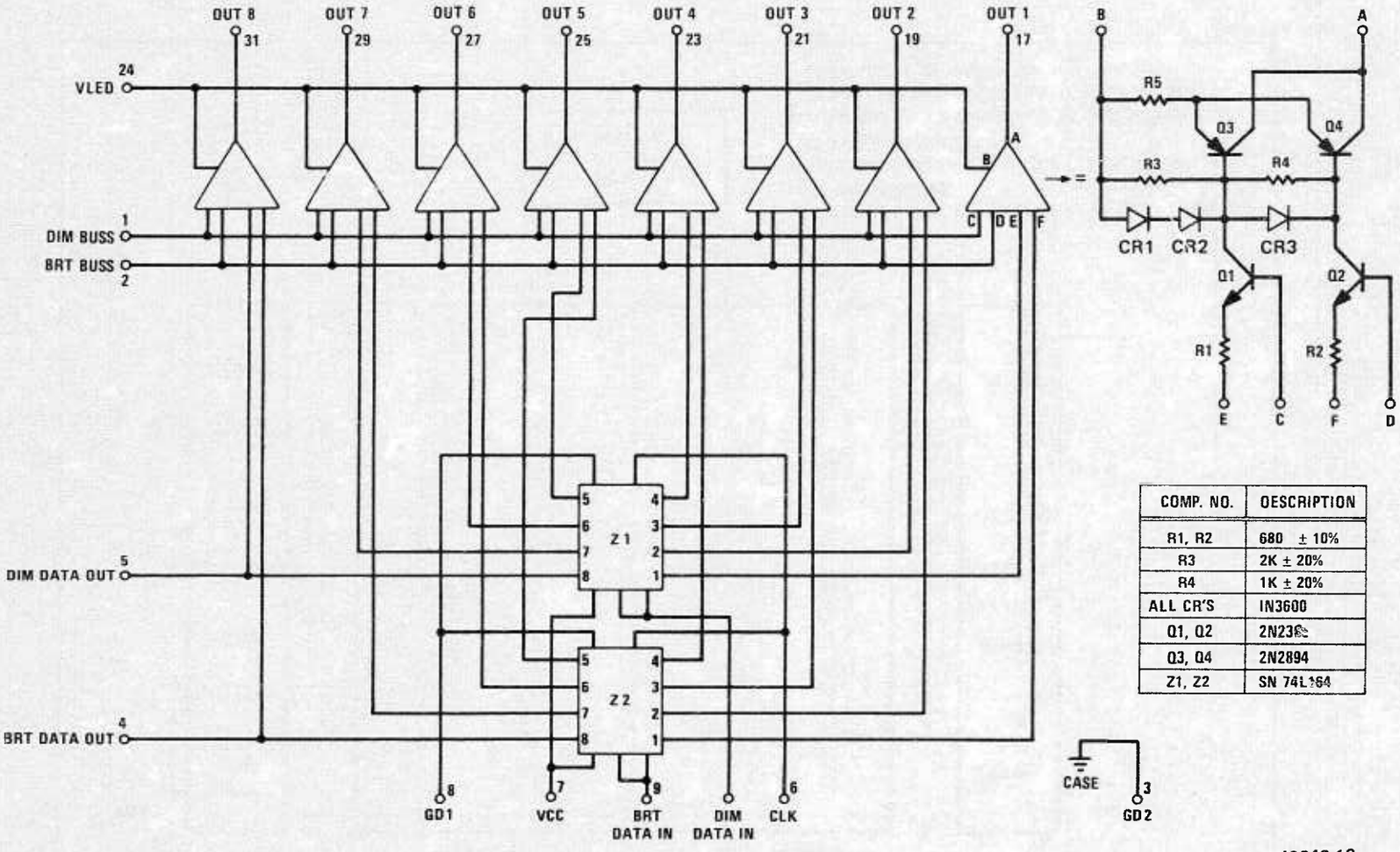


Figure 13. Organization of 1/2-inch by 1/2-inch LED substrate.



COMP. NO.	DESCRIPTION
R1, R2	680 ± 10%
R3	2K ± 20%
R4	1K ± 20%
ALL CR'S	IN3600
Q1, Q2	2N2369
Q3, Q4	2N2894
Z1, Z2	SN 74L164

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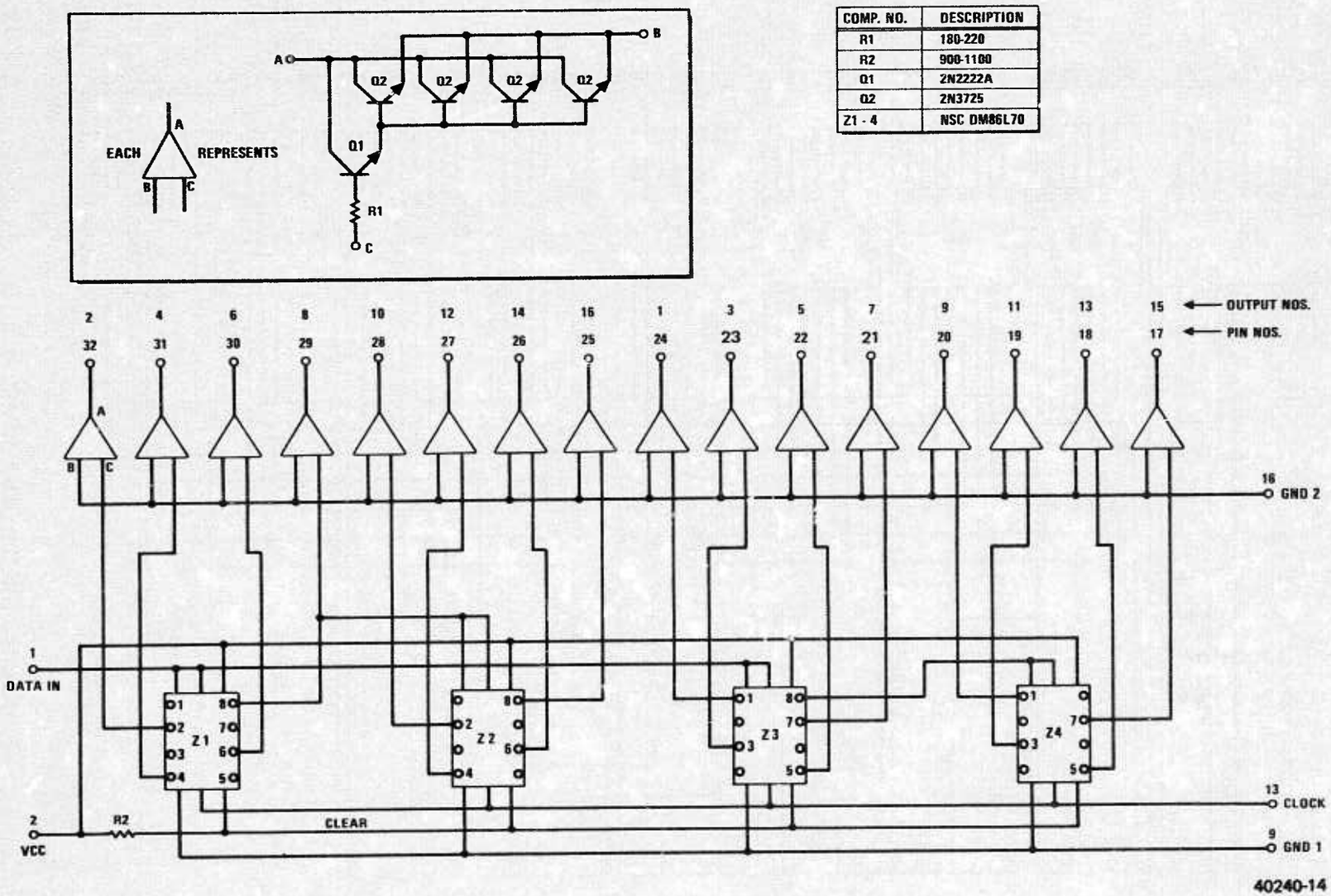
Figure 14. MC1045 row driver hybrid.



COMP. NO.	DESCRIPTION
R1	180-220
R2	900-1100
Q1	2N2222A
Q2	2N3725
Z1 - 4	NSC DM86L70

Figure 15. MC1044 column switch hybrid.

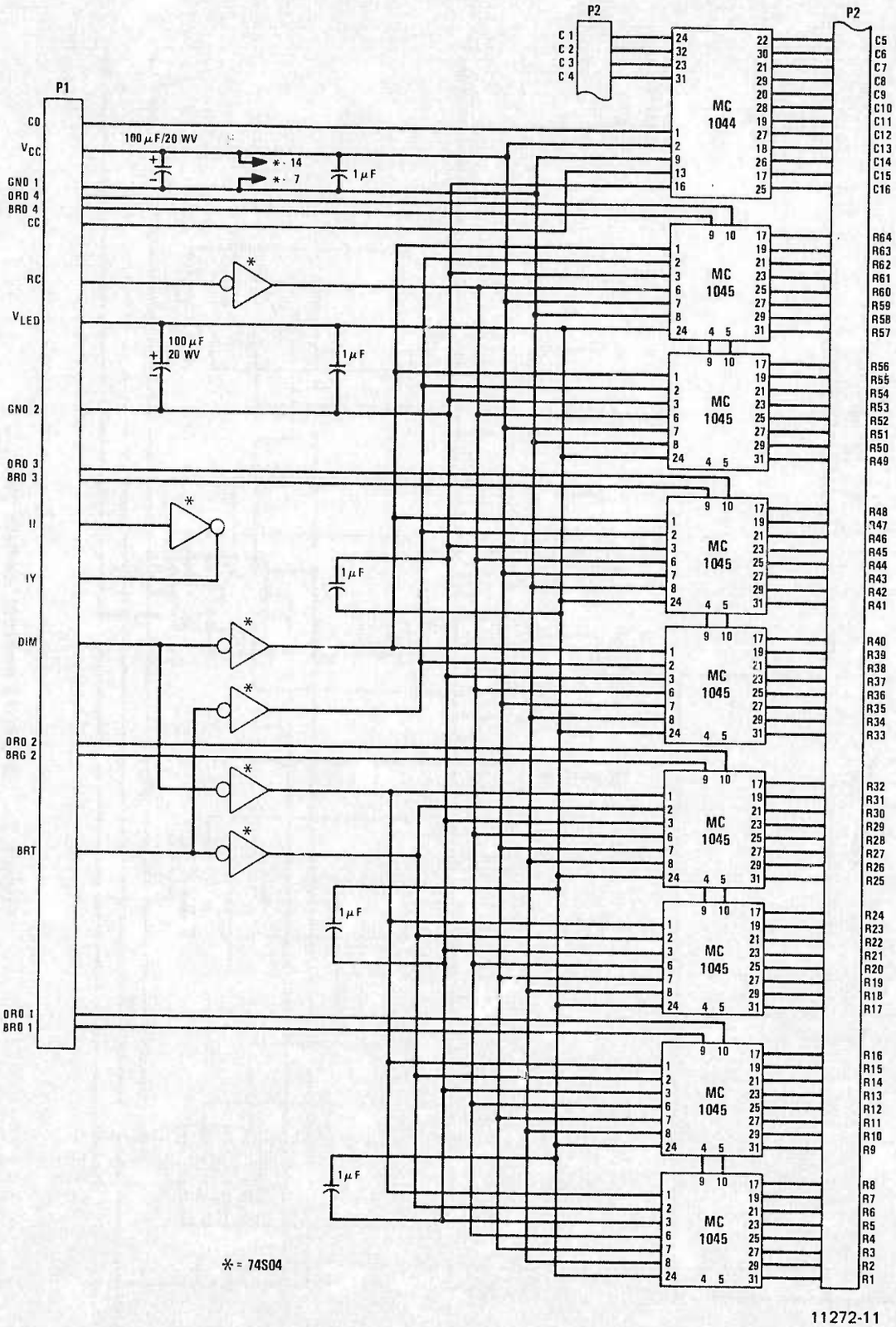


Figure 16. Display head driver card.

The scanning system operates in the following manner: The basic clock in the display operates at 4 MHz with 250 nanoseconds between clocks and all operations in the module are based on this 4 MHz clock. Sixteen bits of video are loaded into the row driver from four ports on the memory. Therefore, 64 bits are loaded in 16 clock times or four microseconds. The column switch is then turned on to display that column of information for 256 clock times or 64 microseconds. This process is repeated for the 16 columns of LEDs to give an overall scan time of 1088 microseconds or 919 Hz scan rate. Since each LED can be turned on for 64 microseconds of the 1088 microseconds available, each LED has a maximum duty cycle of 5.9 percent. The 64 microsecond display time is set for the brightest display available and intensity control is accomplished by turning off the drivers at any clock time within the 64 microseconds. A shorter display pulse will result in less light output from the LEDs.

Bright data for the display of alphanumerics and graphics as well as dim data for the background display are both loaded into the same driver and bus selected for display.

Each of the 1/2-inch by 1/2-inch substrates is scanned independently in this manner to produce the full display.

Front switches on the control panel allow selection of any X-Y point on the display to enter data. A paper tape reader is provided to load a simulated EADI type display. A joystick is provided to allow the viewer to simulate aircraft movement and view the movement on the display. (See Appendix A for operating instructions.)

2.6 DISPLAY GENERATOR

The Display Generator is organized as shown in Figure 17. Inputs to the Display Generator consist of synchronous data, control signals, and asynchronous data.

Each item in the list of synchronous data to be processed is a single word that is clocked in by, and hence synchronous to, an "advance list" control pulse. Each data list item consists of the following parts:

a. Initial X position.

b. Initial Y position.

c. Slope if vector/ASCII code if character.

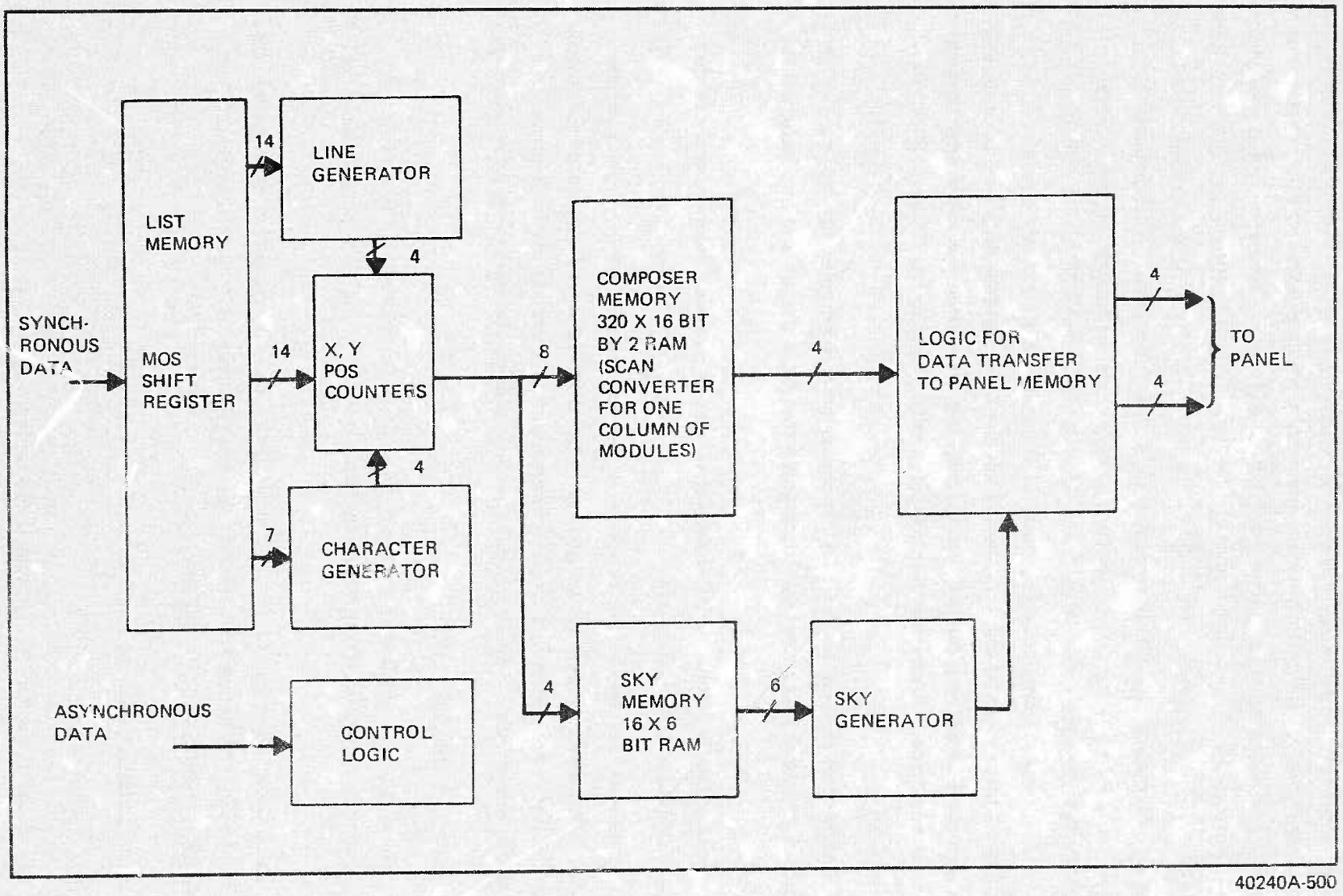


Figure 17. DISPLAY generator.

d. Length, if vector.

e. Accumulator initialization, if vector.

f. Vector/character mode select.

g. Horizon line identifier.

The three control signals that are used to synchronize operation are as follows:

a. Advance List - which causes synchronous data to be clocked into the list memory.

b. Process List - which commands the display generator to initiate its processing and plotting.

c. List Available - which informs the external source of data that list processing is complete and the list memory is available for loading.

The asychronous data lines set the mode of operation of the list processor in the following ways:

a. They allow the refresh memory to be plotted on an item-by-item basis or totally rewritten.

b. They determine whether an item-by-item plot is to be written in the dim or bright sections of the refresh memory.

c. They determine whether the plots into the refresh memory shall be "writes" or "erases."

d. They select either a 5-dot-by-7-dot single-size character or a double (10-dot by 14-dot) plot.

e. They allow the entire refresh memory to be erased or cleared in one cycle.

With reference to Figure 17, the list memory is a MOS shift register and associated control logic that will accept up to 80 items for processing. The list memory control logic keeps track of the number of items loaded by the external data source and sequentially processes each item in the list for each strip in the display. The list memory is completely processed in each strip (with any incomplete partial results returned to the list) before the display generator advances to the next strip.

In processing vector items, the rate multiplier contained in the Line Generator repeatedly adds the slope data to the accumulator value. Whenever a carry occurs, a count is added to either the "x" or the "y" position counters as determined by the control logic. In this way, a vector of any slope may be generated. A length counter counts along with the rate multiplier and may be preset to paint a line one dot long (point plot) or a line going completely across the screen.

When the list item calls for the generation of a character, the character generator takes command of the x and y position counters, stepping them through the character dot matrix. The slope data in the list item is utilized for the ASCII code of the desired character. The character generator font read-only memory determines which points in the matrix are to be illuminated and plots these locations into the compose memory under the control of the asynchronous data specification of matrix size (5 by 7 or 10 by 14).

All character and vector items are plotted into a two-section, 10,240-bit compose memory. Each section has 5,120 locations to represent the diodes in a 5-inch high by 1/4-inch wide display strip. Two identical memory sections are used to allow the simultaneous plotting of data into one section while the other is being destructively read into the main refresh memory.

Any list item that is identified as a "horizon line" has its dot coordinate plotted into a sky memory simultaneously with the item's plot into the compose memory. The sky generator then plots a "wash" of locations to be illuminated into the dim channel of the refresh memory while the compose memory is plotting the bright refresh memory. The sky memory like the compose memory, is divided into two identical halves to allow the simultaneous writing of one strip while reading out into another.

2.7 DISPLAY PROCESSOR

The Display Processor uses 16-bit data words and 40-bit instruction words. For instruction words, 256 program locations are available while 18 data word storage registers are provided. A Programmable Read-Only-Memory (PROM) provides 128 sixteen-bit storage of constants to be used by the program. Negative numbers are represented in two's complement form.

Figure 18 shows the major blocks of the Display Processor as they are related by data transfer paths. Control signals for each block (e.g., addressing of register files) are derived from dedicated fields in the instruction word, as described below.

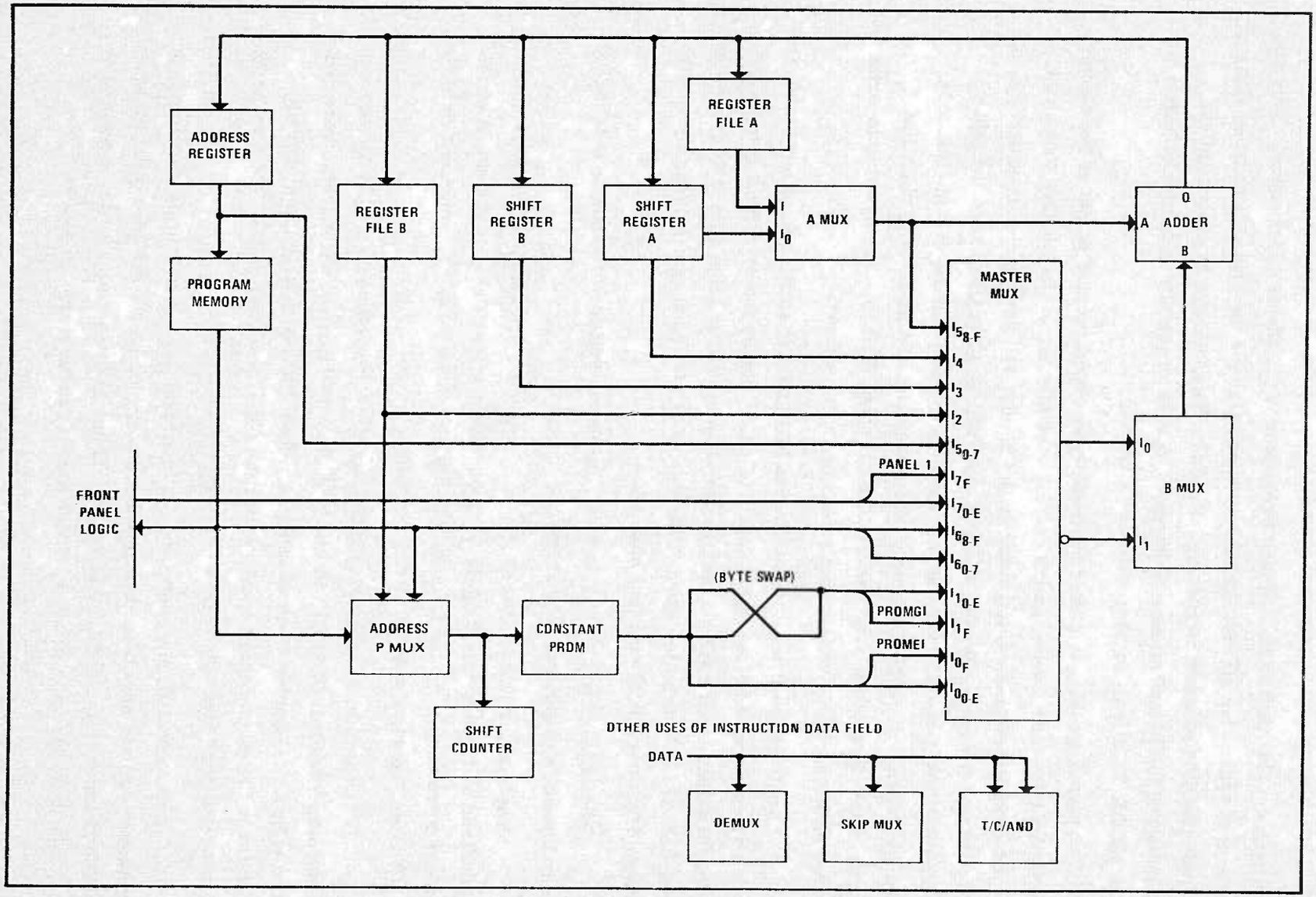


Figure 18. Display processor data flow diagram.

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The primary data path in the Display Processor is the 16-bit adder output. This bus is the data source for all storage registers and also for the program address register, thereby enabling program branching. Inputs to the adder are the A-multiplexer (A-mux) and the B-multiplexer (B-mux). The A-mux permits selection of either register file A (File A) or shift register A (SRA).

The B-mux selects either the true or the complemented output of the master multiplexer (M-mux), which is the central data selector in the Display Processor. By selecting the complemented output of the M-mux and forcing the input carry of the adder to '1', the input selected at the M-mux will be subtracted from the input selected by the A-mux. Two register files (File A and File B) provide the main Display Processor working storage. Each register file consists of eight 16-bit words, with independent read and write addressing (that is, it is possible to write in one location while simultaneously reading from another).

Two 16-bit shift registers (SRA and SRB) permit shifting in several modes which are described below. Shift length is controlled by the 4-bit shift counter, which is loaded via the PROM multiplexer (P-mux) either from File B or from the data field of the instruction word. The P-mux is also used to select the addressing source from the PROM constant memory.

The address register is an 8-bit, up/down counter which can be side loaded from the adder output bus for branching.

The program memory contains 256 forty-bit instruction words; it is directly addressed by the Address Register. Decodes of various fields in the output of the program memory are used to control the other blocks (e.g., M-mux input selection, shift mode, address register count direction, etc.).

The operational program for the Display Processor is given in Appendix B. The column headed 'OBJECT' in Appendix B is the hexadecimal machine code generated by an assembler from an input card deck containing only the mnemonic entries in the other columns, along with the free-form comments. The flow chart of this operational program is given in Appendix C.

In Appendix B, the Name and AD (address) fields are merely aids to the programmer and are not utilized by the assembler; comments for each instruction are listed at the extreme right. The other columns in the listing are interpreted by the assembler as shown in Table 1, where the bit numbers are hexadecimal.

TABLE 1. INSTRUCTION WORD FIELDS (SHEET 1 OF 7)

Bits	Field
27	Advance
26	
25	
24	AMUX
23	
22	Skip MUX
21	
20	
1F	Shift
1E	
1D	
1C	
1B	Discrete Demux Enable
1A	Master MUX
19	
18	
17	Address MUX
16	File A Read
15	
14	
13	Carry
12	File B Read
11	
10	
0F	File Write
0E	
0D	
0C	
0B	(C)
0A	Mask
09	
08	
07 ↓	Data
00	

TABLE 1. INSTRUCTION WORD FIELDS (SHEET 2 OF 7)

Advance Field				
Bit			Mnemonic	Action
27	26	25		
0	0	0	AD	Advance IF
0	0	1	SK	Skip IF
0	1	0	BK	Back IF
0	1	1	DO	DO IF
1	0	0	AD, N	Advance IF NOT
1	0	1	SK, N	Skip IF NOT
1	1	0	BK, N	Back IF NOT
1	1	1	DO, N	DO IF NOT

A MUX Field			
Bit		Mnemonic	Action
24	23		
0	0	SRA	Shift Register A
0	1	FLA	File A
1	0	(Not Used)	
1	1	(Default)	0

Skip Field				
Bit			Mnemonic	Action
22	21	20		
0	0	0	JMIN	Minor MUX
0	0	1	JSTC	Shift TC
0	1	0	JEAD	EADI Mode
0	1	1	JEOQ	End of Sequence
1	0	0	JQMS	Q MSB
1	0	1	JCAR	Carry
1	1	0	JZED	Zero Detect
1	1	1	(Default)	1

TABLE 1. INSTRUCTION WORD FIELDS (SHEET 3 OF 7)

Shift Field					
Bit				Mnemonic	Action
1F	1E	1D	1C		
0	0	0	0	SLLG	Shift Left Logical
0	0	0	1	SRLG	Shift Right Logical
0	0	1	0	SLEA	Shift Left End-around
0	0	1	1	SRAR	Shift Right Arithmetic
0	1	0	0	SLGK	Shift Left Logical Linked
0	1	0	1	SREL	Shift Right End-around Linked
0	1	1	0	SLIN	Shift Left End-around Linked (Divide)
0	1	1	1	SRAK	Shift Right Arithmetic Linked
1	0	0	0	LSRA	Load Shift Reg. A
1	0	0	1	LSRB	Load Shift Reg. B
1	0	1	0	LSAM	Load SRA; Multiply
1	0	1	1	LREG	Nothing (Load Reg. File)
1	1	0	0	LSAD	Load SRA; Divide
1	1	0	1	LADD	Nothing (Load Address)
1	1	1	0	LSAG	Load SRA; Load Reg. File
1	1	1	1	LNSN	Nothing

NOTE: See Also Figure 2

Demux Field		
Bit 1B	Mnemonic	Action
0	DE	Active
1	(Default)	Inactive

TABLE 1. INSTRUCTION WORD FIELDS (SHEET 4 OF 7)

Master MUX Field

Bit 1A	Bit 19	Bit 18	Mnemonic	Action	Note
0	0	0	MPRM	Prom	1
0	0	1	MPRS	Prom Swap	2
0	1	0	MFLB	File B	
0	1	1	MSRB	Shift Reg. B	
1	0	0	MSRA	Shift Reg. A	
1	0	1	MADD	Address Cntr/File A LSBs	
1	1	0	MDTF	Data Field	
1	1	1	MPAN	Panel	1

NOTES: 1. E Bit is copied into F Bit.
2. 6 Bit is copied into F Bit.

Address MUX Field

Bit 17	Mnemonic	Action
0	AMPG	Program
1	AMFB	File B

File A Field

Bit 16	Bit 15	Bit 14	Mnemonic	Action
0	0	0	RA0	Read Reg. A0
0	0	1	RA1	Read Reg. A1
0	1	0	RA2	Read Reg. A2
0	1	1	RA3	Read Reg. A3
1	0	0	RA4	Read Reg. A4
1	0	1	RA5	Read Reg. A5
1	1	0	RA6	Read Reg. A6
1	1	1	RA7	Read Reg. A7

TABLE 1. INSTRUCTION WORD FIELDS (SHEET 5 OF 7)

Carry Field

Bit 13	Mnemonic	Action
0	CR1	Active
1	(Default)	Inactive

File B Field

Bit 12	Bit 11	Bit 10	Mnemonic	Action
0	0	0	RB0	Read Reg. B0
0	0	1	RB1	Read Reg. B1
0	1	0	RB2	Read Reg. B2
0	1	1	RB3	Read Reg. B3
1	0	0	RB4	Read Reg. B4
1	0	1	RB5	Read Reg. B5
1	1	0	RB6	Read Reg. B6
1	1	1	RB7	Read Reg. B7

File Write Field

Bit OF	Bit OE	Bit OD	Bit OC	Mnemonic	Action
0	0	0	0	WA0	Write Reg. A0
0	0	0	1	WA1	Write Reg. A1
0	0	1	0	WA2	Write Reg. A2
0	0	1	1	WA3	Write Reg. A3
0	1	0	0	WA4	Write Reg. A4
0	1	0	1	WA5	Write Reg. A5
0	1	1	0	WA6	Write Reg. A6
0	1	1	1	WA7	Write Reg. A7

TABLE 1. INSTRUCTION WORD FIELDS (SHEET 6 OF 7)

File Write Field (cont)

Bit OF	OE	OD	OC	Mnemonic	Action
1	0	0	0	WB0	Write REG B0
1	0	0	1	WB1	Write REG B1
1	0	1	0	WB2	Write REG B2
1	0	1	1	WB3	Write REG B3
1	1	0	0	WB4	Write REG B4
1	1	0	1	WB5	Write REG B5
1	1	1	0	WB6	Write REG B6
1	1	1	1	WB7	Write REG B7

Mask Field

Bit OB	OA	09	08	Mnemonic	Action
0	0	0	0	(Not Used)	
0	0	0	1	(Not Used)	
0	0	1	0	BMA0, C	Comp, upper and, 0 lower
0	0	1	1	BMA1, C	Comp, upper and, 1 lower
0	1	0	0	BM0A, C	Comp, lower and, 0 upper
0	1	0	1	BM1A, C	Comp, lower and, 1 upper
0	1	1	0	ZERO, C	Comp, 0
0	1	1	1	(Default), C	Comp, pass
1	0	0	0	(Not Used)	
1	0	0	1	(Not Used)	
1	0	1	0	BMA0	True, upper and, 0 lower
1	0	1	1	BMA1	True, upper and, 1 lower
1	1	0	0	BM0A	True, lower and, 0 upper
1	1	0	1	BM1A	True, lower and, 1 upper
1	1	1	0	ZERO	True, 0
1	1	1	1	(Default)	True, pass

TABLE 1. INSTRUCTION WORD FIELDS (SHEET 7 OF 7)

Data Field									
Bit									
07	06	05	04	03	02	01	00	Mnemonic	Action
*	*	*	*	*	*	*	*	**	See Table 2

*The two characters of the mnemonic will be 0-F, indicating in order the upper 4 bits and the lower 4 bits of the data field.

The Advance Field (Table 1, page 42) operates with the Skip Field (Table 1, page 42) to determine program flow. "Advance If" means increment the program address register by one if the condition specified by the Skip Field is true ('1'). Note that the Skip Field includes a forced true condition, providing an unconditional advance. "Skip If" causes the next instruction not to execute its function if the Skip Field condition is true; the address register will simply count through to the instruction following. "Back If" decrements the address counter by one if the Skip condition is true; otherwise, the counter increments by one. The instruction executes in either case. (Note that the alternatives with "AD" are count up or not at all, while with "BK", they are count down or count up.) "Do If" increments the program address counter by one; the instruction is executed if the Skip Condition is true. The 'not' (N) qualifier simply inverts the sense of the Skip Condition.

The A-MUX Field (Table 1, page 42) selects either SRA or File A for the A input of the adder; if neither is selected, the output of the A-mux is forced to zero.

The Skip Field selects the condition to be tested for truth by the address control logic to determine program flow. One of these conditions is the forced '1' mentioned above. Another is the terminal count (TC) of the shift counter, which provides the means of shifting a specified number of places in one instruction by using the "Advance If" code. The shift instruction will be executed once for each clock, but the address will not advance until the shift counter TC is true, whereupon the address counter will advance to the next instruction. The "Minor Mux" serves as an expansion of the Skip Mux, providing access to six (of eight) sense switches and two external control signals. Other conditions in the Skip Field are described in Table 1.

The Shift Field (Table 1, page 43) controls the shift mode of SRA and SRB as shown in Figure 19 and also controls the loading of SRA, SRB, the address counter, File A, and File B. (File addresses for writing are controlled by the File Write Field discussed below.) Four different codes can cause SRA to be loaded; they control other functions in different ways. LSRA only loads SRA, with no other unique control; LSAM loads SRA and additionally controls the multiplication algorithm. LSAD, in addition to loading SRA, controls the division algorithm. LSAG loads both SRA and File A or B, simultaneously. LADD loads the address counter, causing a branch. Finally, if the field is specified with LNSN (or not specified at all, a default condition), the assembler will generate object code of 1111, the 'no-op' code; the Shift Field will not cause any action in the instruction.

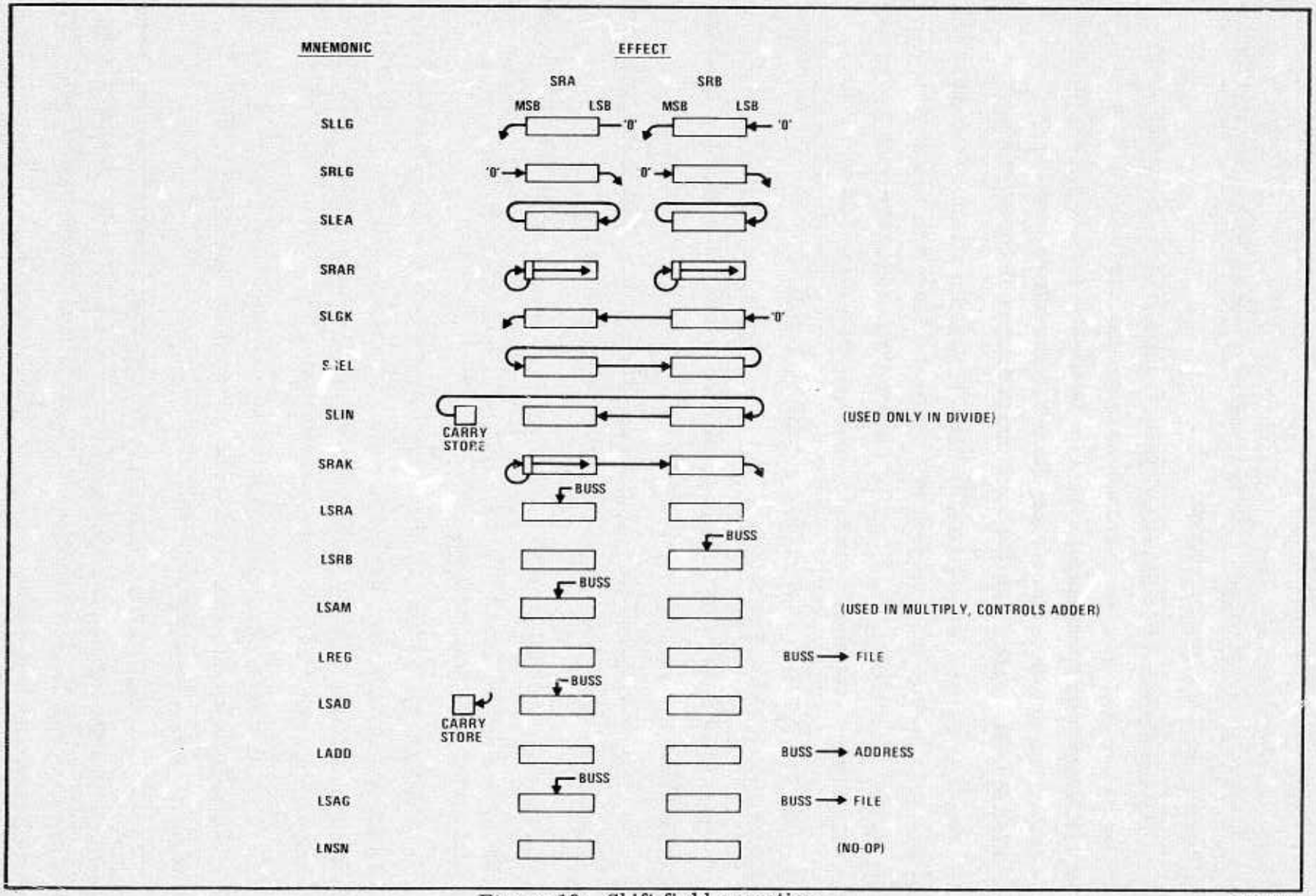

Figure 19. Shift field operation.

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The Discrete Demux Field ('DX') (Table 1, page 43) generates one bit of object code. If DE is specified, the Demux is active and performs the function specified by bits 4, 5, and 6 in the data field. If DI is specified or the entry is blank, the Demux performs no function in the instruction.

The Master Mux Field ('MMUX') (Table 1, page 44) selects the data source for the B input channel of the adder. Prom Swap means that the two bytes from the Constant PROM are to be interchanged. When the instruction word Data Field is specified, it is entered twice, both in bits 0-7 and bits 8-F. The output of the Master Mux is further affected by the Mask Field of the instruction word as discussed below.

The Address Mux Field ('ADMX') (Table 1, page 44) selects either the instruction word Data Field or the LS byte of File B, via the Prom Mux, to address the Constant PROM. Additionally, the 4 LSBs of the Prom Mux output are compared against the Shift Counter to establish Terminal Count, one of the Skip Field conditions.

The File A Field ('FLA') (Table 1, page 44) simply addresses (for reading) one of eight data words stored in File A.

The Carry Field ('CRY') (Table 1, page 45) selects the state of the input carry bit of the adder.

The File B Field ('FLB') (Table 1, page 45) selects the File B word to be read in exactly the same manner as the File A Field addresses File A.

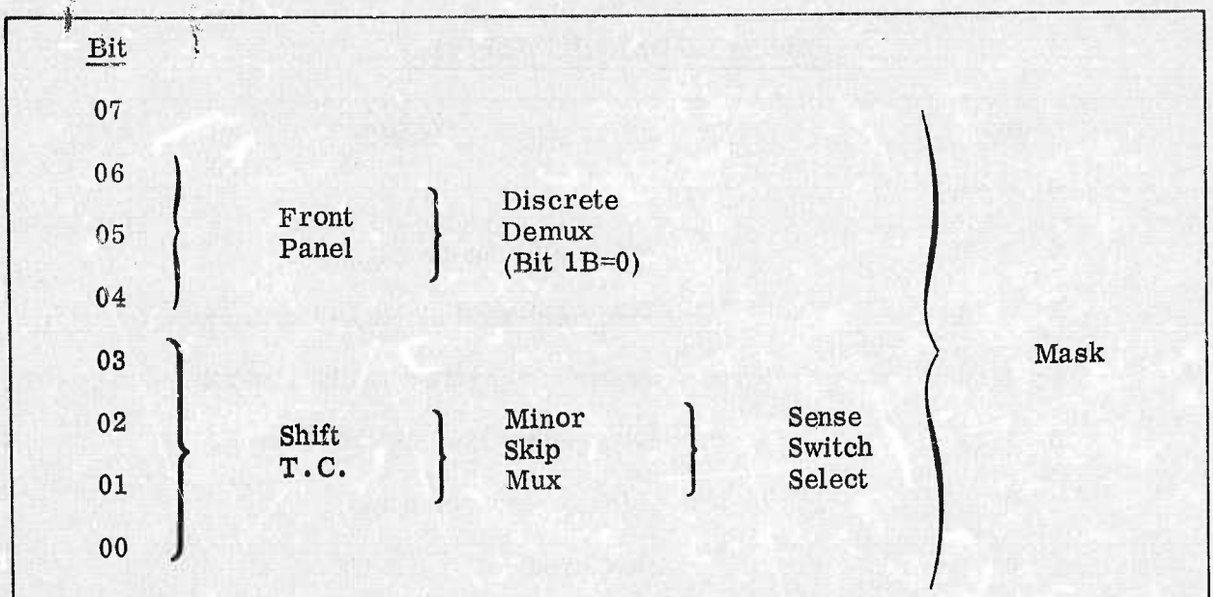
The File Write Field ('FWT') (Table 1, page 45) controls the write addressing for both File A and File B. Note that the Shift Field must specify that a Register File is to be loaded for writing to occur (LREG or LSAG).

The Mask Field (Table 1, page 46) applies the Data Field to either the MS byte or the LS byte of the Master Mux, performing a bit-by-bit AND; the other byte of the Master Mux is forced to either 1's or 0's. Finally, the Mask Field controls the B-mux to select either the true or the complemented output of the Master Mux.

The Mask Field (Table 1, page 46) can also be programmed to pass the Full Master Mux selected input data word in either true or complemented form, or to force the B input of the adder to be either all 1's or all 0's.

The Data Field (Table 2, page 51) performs several different functions in conjunction with other fields of the instruction word. The most basic function is simply as a raw source of data to be used as an operand in an arithmetic instruction. The other functions are as follows:

TABLE 2. DATA FIELD SUBFIELDS (SHEET 1 OF 3)



FRONT PANEL SUBFIELD

Bit	Data Item
6 5 4	
0 0 0	X Initial
0 0 1	Y Initial
0 1 0	X Final
0 1 1	Y Final
1 0 0	A/N #1
1 0 1	A/N #2
1 1 0	Theta (Pitch Angle)
1 1 1	Phi (Roll Angle)

TABLE 2. DATA FIELD SUBFIELDS (SHEET 2 OF 3)

DISCRETE DEMUX SUBFIELD

Bit	Action
6 5 4	
0 0 0	Reset all sense switches
0 0 1	Reset selected sense switch (Note 2)
0 1 0	Set selected sense switch (Note 2)
0 1 1	Store adder bus MSB (QMSB)
1 0 0	Advance list command
1 0 1	(Not used)
1 1 0	Front panel data request
1 1 1	Process list command

NOTES: 1. These actions occur only when bit 1B is zero.

2. See Table 2, sheet 3.

SHIFT T.C. SUBFIELD

Bit	Action
3 2 1 0	
0 0 0 0	Shift one place
0 1 0 1	Shift six places
1 1 1 1	Shift sixteen places

TABLE 2. DATA FIELD SUBFIELDS (SHEET 3 OF 3)

MINOR SKIP MUX SUBFIELD	
Bit 2 1 0	Condition Tested (if bits 20, 21, 22 = 0)
0 0 0	Sense Switch 0
0 0 1	Sense Switch 1
0 1 0	Sense Switch 2
0 1 1	Sense Switch 3
1 0 0	Sense Switch 4
1 0 1	Sense Switch 5
1 1 0	Front Panel Data Ready
1 1 1	List Process Complete

SENSE SWITCH SELECT SUBFIELD		
Bit 2 1 0	Selected Sense Switch	
0 0 0	0	
0 0 1	1	
0 1 0	2	
0 1 1	3	[Switch will be set or reset according to discrete demux subfield (see Table 2, sheet 2)]
1 0 0	4	
1 0 1	5	
1 1 0	6	
1 1 1	7	

a. Address for branch instructions (load address register from Data Field).

b. Define terminal count for shift instructions.

c. Minor Skip Mux Selection (bits 0, 1, 2). The Minor Skip Mux is functionally just an expansion of the main Skip Mux; when the main Skip Mux Field (bits 20, 21 22) selects the Minor Skip Mux, the Data Field completes the selection. Eight Sense Switches can be set and reset under program control, and six of these are made available via the Minor Skip Mux as conditions to be tested for control in the Advance logic. Two external lines are also provided through the Minor Skip Mux. One line is from the Front Panel logic signifying that new input data is ready and the other line is from the Display Generator signifying that it is ready to accept a new list of display items.

d. Discrete Demux Select. When the Discrete Demux is active (Bit 1B), bits 4, 5, and 6 of the Data Field are decoded to drive one of seven control lines. These controls are defined in Table 2.

e. Sense Switch Select. Bits 0, 1, and 2 are used to select which Sense Switch will be set or reset by the Discrete Demux when active.

f. Front Panel Address. Bits 4, 5, and 6 are used to address storage registers in the Front Panel logic to request specific data items such as pitch or roll angle.

g. B Operand Mask. The entire data field is used in conjunction with the Mask Field to modify the B input of the adder via the Master Mux and the B-mux.

The front panel logic of the Display Processor interfaces the joystick and front panel switches or the tape reader to the Display Processor via the format shown in Figure 20. The "address" shown in Figure 20 is bits 4, 5, and 6 of the Data Field of the instruction word (see Table 2) when the Master Mux Field is all 1's ('MPAN'). In order to read data from the front panel, the Display Processor first issues a "Front Panel Data Request" via the Discrete Demux. This commands the panel logic to scan the joystick and data switches, storing their outputs in designated registers. Upon completion of this scan, the panel logic returns a "Front Panel Data Ready" signal to the Minor Skip Mux. The Display Processor, when it senses this signal, can read the new data to update the display.

MUX CODE	F E	D	C	B	A												DATA LINES
	15 14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
0 0 0	ROLL	X INITIAL									O						
0 0 1	PITCH	Y INITIAL									O						
0 1 0	AN	X FINAL									O						
0 1 1	1	Y FINAL									O						
1 0 0	0 0 0	AN1									O						
1 0 1	0 0 0	AN2									O						
1 1 0	0	Θ															
1 1 1	0	Φ															
	STOP MUX 15 14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		MASTER MUX

NOTES: ALL INPUTS ARE 2's COMPLEMENT WITH BINARY POINT AS INDICATED.
Θ AND Φ RANGE FROM 0.0 TO 359.984375. AN1 AND AN2 ARE ASCII.

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Figure 20. Display processor front panel inputs.

The Display Processor transmits 43 bits of data to the Display Generator for each display item: Sense Switches 0, 3, 4, 5, and 6; File words A5 (15 bits: 0-6 and 8-F) and B7 (7 bits: 1-7); and SRB (16 bits). The Display Generator is triggered to accept the data by an Advance List command from the Discrete Demux. After the last item in an update cycle has been sent, the Display Processor issues a Process List command via the Discrete Demux to the Display Generator. When the Display Generator receives the Process List command, it drops its Ready line; this condition is recognized by the Minor Skip Mux as List Processed = False and is used by the Display Processor to halt update processing until the Display Generator has fully updated the Refresh Memory from the last list of items transmitted. When the Display Generator completes its update, List Processed = True, and the DP is released to process a new input from the front panel. Table 3 shows the data formats used to send lines and alphanumerics to the Display Generator.

Table 4 lists the constants that are stored in the PROM.

TABLE 3. DISPLAY PROCESSOR OUTPUT DATA FORMATS

Sense Switch 0		'0' - not horizon; '1' - horizon line	
Sense Switch 3		'0' - line; '1' - alphanumeric	
Sense Switch 4		'0' - line has + slope; '1' - line has - slope	
Sense Switch 5		'0' - line is $> 45^{o}$ from horizontal	
		'0' - line is $< 45^{o}$ from horizontal	
Sense Switch 6		'0' - sky below horizon (e.g., inverted flight)	
		'1' - sky above horizon	
File A5-bit	F	MSB	Y Position
	bit 8	LSB	
	bit 6	MSB	X Position
	bit 0	LSB	
File B7-bit	7		Length of line
	bit 1		
SRB -	bit F		Slope of line or A/N ASCII Code
	bit 8		
	bit 7		Accumulator (initialization constant, dependent upon pitch and roll angles, required by Display Generator)
	bit 0		

TABLE 4. PROM CONSTANTS FOR DISPLAY PROCESSOR OPERATIONAL PROGRAM

00	0D48	20	7680	40	*	60	*
01	0705	21	6B00	41	*	61	*
02	0390	22	7880	42	*	62	*
03	01CA	23	6A00	43	*	63	*
04	00E5	24	7A80	44	7000	64	*
05	0073	25	6100	45	7B00	65	*
06	0039	26	1E80	46	0500	66	*
07	001D	27	*	47	1000	67	*
08	000E	28	*	48	707F	68	*
09	0007	29	*	49	7B7F	69	*
0A	0004	2A	*	4A	057F	6A	*
0B	0002	2B	*	4B	107F	6B	*
0C	0001	2C	*	4C	7F01	6C	*
0D	8000	2D	8	4D	0101	6D	*
0E	00BB	2E	*	4E	7F00	6E	*
0F	26DD	2F	*	4F	0100	6F	*
10	001B	30	*	50	7F7F	70	*
11	0044	31	*	51	017F	71	*
12	000A	32	*	52	7A7C	72	*
13	000A	33	*	53	7A7E	73	*
14	0005	34	*	54	7B7C	74	*
15	0080	35	*	55	7B7E	75	*
16	FFF1	36	*	56	057C	76	*
17	2300	37	*	57	057E	77	*
18	0007	38	*	58	067C	78	*
19	0061	39	*	59	06FE	79	*
1A	0500	3A	*	5A	*	7A	*
1B	6900	3B	*	5B	*	7B	*
1C	7280	3C	*	5C	*	7C	*
1D	6800	3D	*	5D	*	7D	*
1E	7480	3E	*	5E	*	7E	2D00
1F	6300	3F	*	5F	*	7F	1680

* = Not used.

SECTION 3

EVALUATION OF MONOLITHIC LED ARRAYS

The electrical properties of the monolithic LEDs produced in this program and described in Section 2 are similar to those observed in discrete devices. The forward and reverse characteristics of a single emitter measured on a completed array, as well as the electrical properties of the isolation diffusion channels, are illustrated in Figure 21. Curve A-B shows the nominal characteristic of a single emitter p-region measured with respect to an n-contact on the same isolation channel. Curve B-C shows the I-V characteristic of the n-channel isolation diffusions and the buried grown junction. As can be seen, these junctions provide exceptionally high impedance in reverse bias with breakdown voltages in the range of 30 to 50 volts and leakage currents of less than 10^{-8}A. Finally, curve B-B' shows the resultant electrical isolation between two adjacent n-type channels, exhibiting the same low values for leakage current.

Single emitter I-V characteristics are given in more detail in Figure 22. Since these forward voltages were measured using pressure contacts they may be a bit higher than would be obtained with a bonded lead. Other variations in the I-V characteristics are caused by variation of spreading resistance around the contacts. This also causes nonuniform brightness across the LED which is examined below. The nonuniformity is not readily visible in normal viewing.

The optical performance of these arrays as viewed either from the active side or through the substrate is illustrated in Figures 23 and 24, respectively. Figure 23 shows photographs of an array mounted in a 14-pin dual in-line ceramic package which is operating in normal laboratory ambient light (Figure 23A) and in zero ambient light (Figure 23B). The array is mounted with the substrate side epoxy bonded to the package and the array rows and columns are wire bonded to the contact pads. The arrays have complete alphanumeric capability. As can be seen in Figure 23, the optical cross-talk between different emitters is minimal and the contrast ratio is fully satisfactory for normal viewing.

A more definitive measurement of the optical performance of an array is shown in Figure 24. In this case the array performance is measured through the substrate side to illustrate the suitability of these devices for flip-chip bonding. As indicated in Figure 24, the contrast ratio was measured by scanning a Gamma Scientific Co. spot

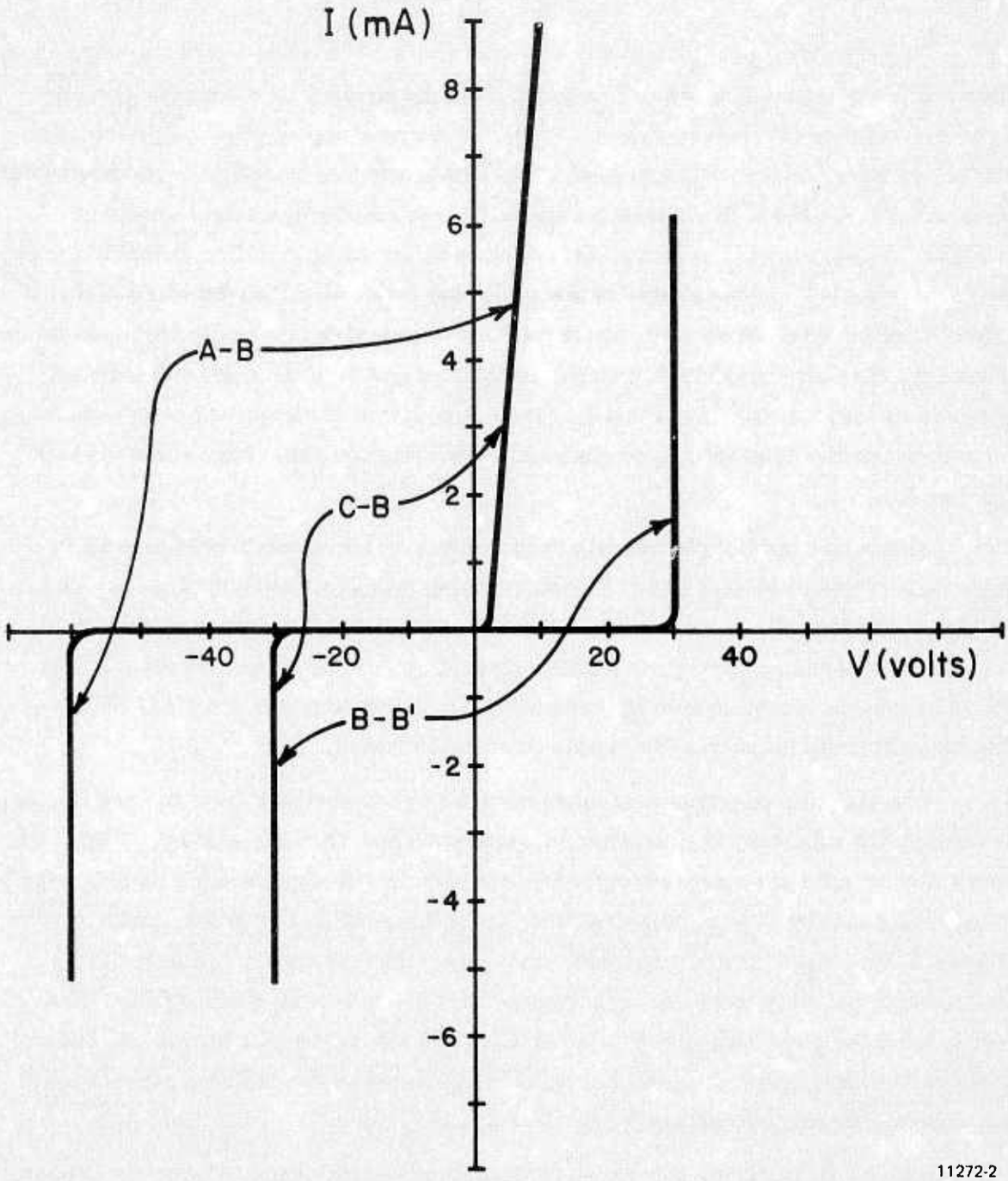


Figure 21. Forward and reverse I-V characteristics of monolithic LEDs.

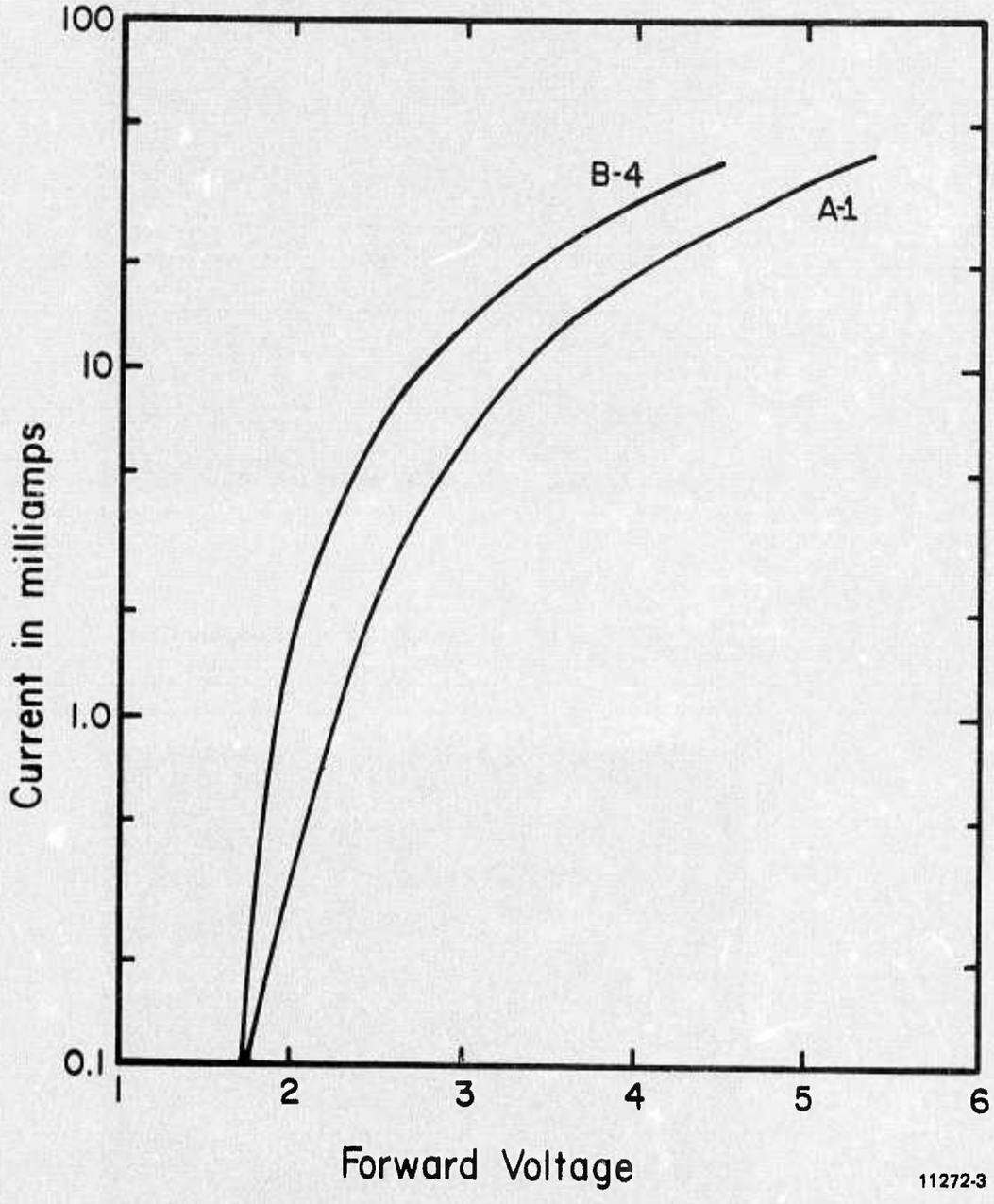
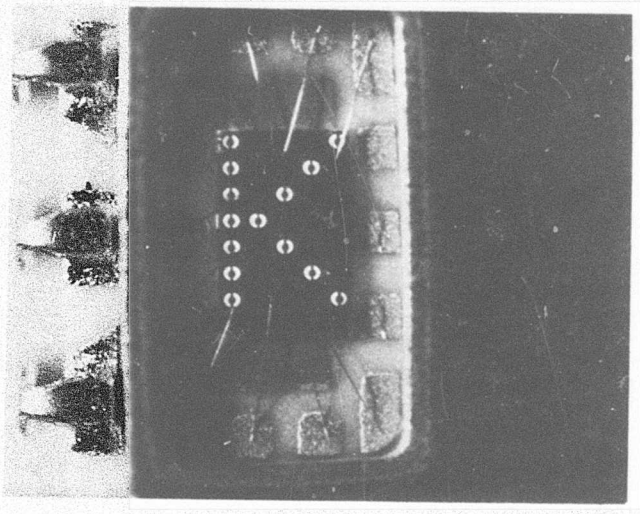
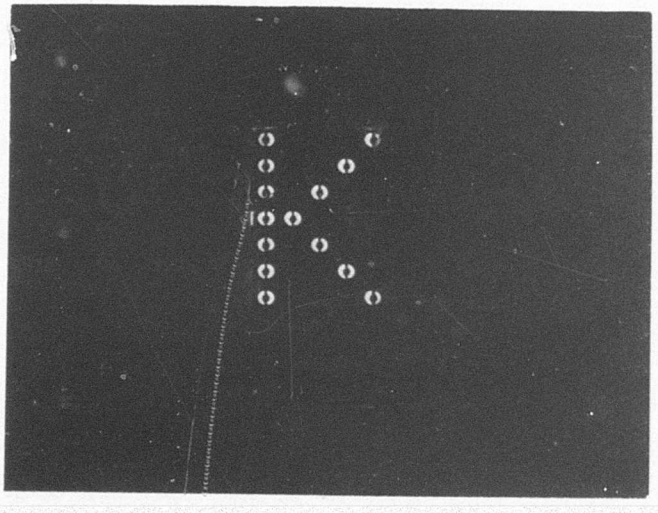


Figure 22. Forward I-V characteristics of single LED junctions.



40240-28

(A) Operating in normal laboratory illumination.



40240-29

(B) Operating in zero ambient light.

Figure 23. 5x7 X-Y addressable array mounted with contact pads up in an 11-pin dual inline package.

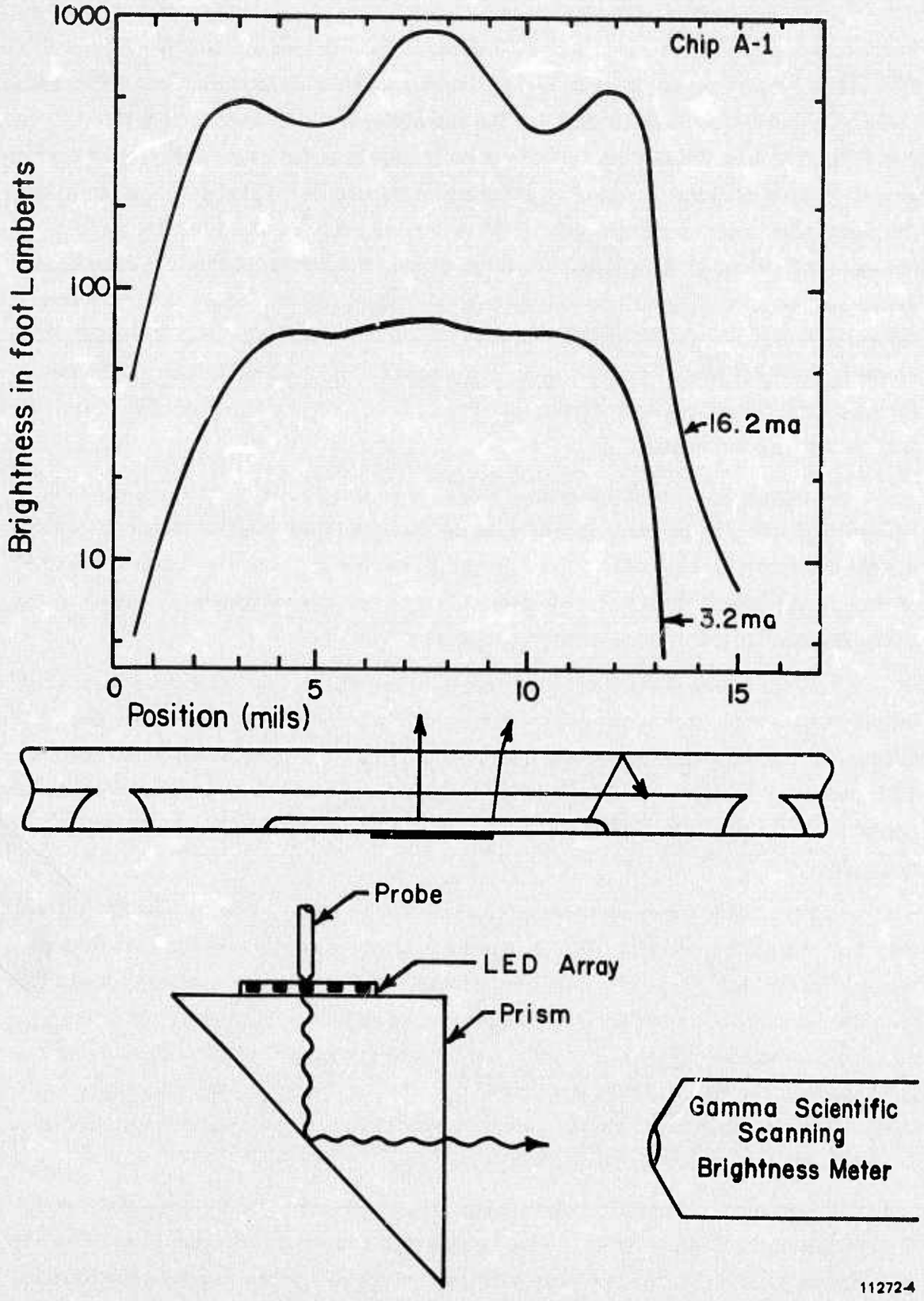


Figure 24. LED junction viewed through substrate.

brightness meter, with a resolution of 0.0015, across the substrate side of the wafer. For viewing convenience, a right angle prism was employed to reflect the array image so that the arrays could be probed and the spotmeter could be used in a horizontal position. The brightness as a function of spotmeter position on an array, with a single emitter region activated, is plotted at the top of Figure 24. This plot is aligned with the schematic cross-sectional view of the array, which has 8 mil emitting regions, shown at the center of Figure 24. The high central brightness at the top of the peak is related to the spreading resistance from the p-contact and the increased brightness at the outside region is related to the nature of the edge of the junction. The latter phenomenon does not occur in all arrays. For example, in Figure 25, there is no increased brightness observed toward the edge of the diode and the spreading of the central contact predominates.

In Figure 24, the effective spot size is seen to be about 10 mils, measured to the one half intensity points. This is roughly the sum of the junction diameter and the sensor diameter which would be the expected result for a uniform source. The type of chip shown in Figure 25 has a smaller effective spot size because the effects of the spreading resistance of the p-contact are more pronounced.

The optical cross-talk of these arrays is minimal. The brightness measured midway between emitter is normally 100X less than at the emitter position. The brightness at a neighboring extinguished LED position is less than that at the operating LED position by a factor of about 200X. The optical cross-talk caused by metallization separated from the GaP by SiO_2 or Si_3N_4 layers or by ohmic contact regions is negligible.

Light can be observed at the edge of a chip, especially when a row of emitters next to that edge are driven. This is caused by the trapping of radiation emitted at angles greater than 17 degrees (the critical angle of GaP for total internal reflection) from the normal to the surface. This radiation is attenuated by absorption in the slice and by transmission through the surface at imperfections and the remainder exits from the sample at the edge. The magnitude of this effect is such that the chip edges are occasionally noticeable to the viewer, but never to the extent that they are distracting or interfere with character recognition.

It is apparent from Figures 24 and 25 that the luminous efficiency of the emitters is superlinear with current. This is shown in a more direct manner in Figure 26. At currents of 16.2 mA the luminous efficiency of these devices ranges from about 20

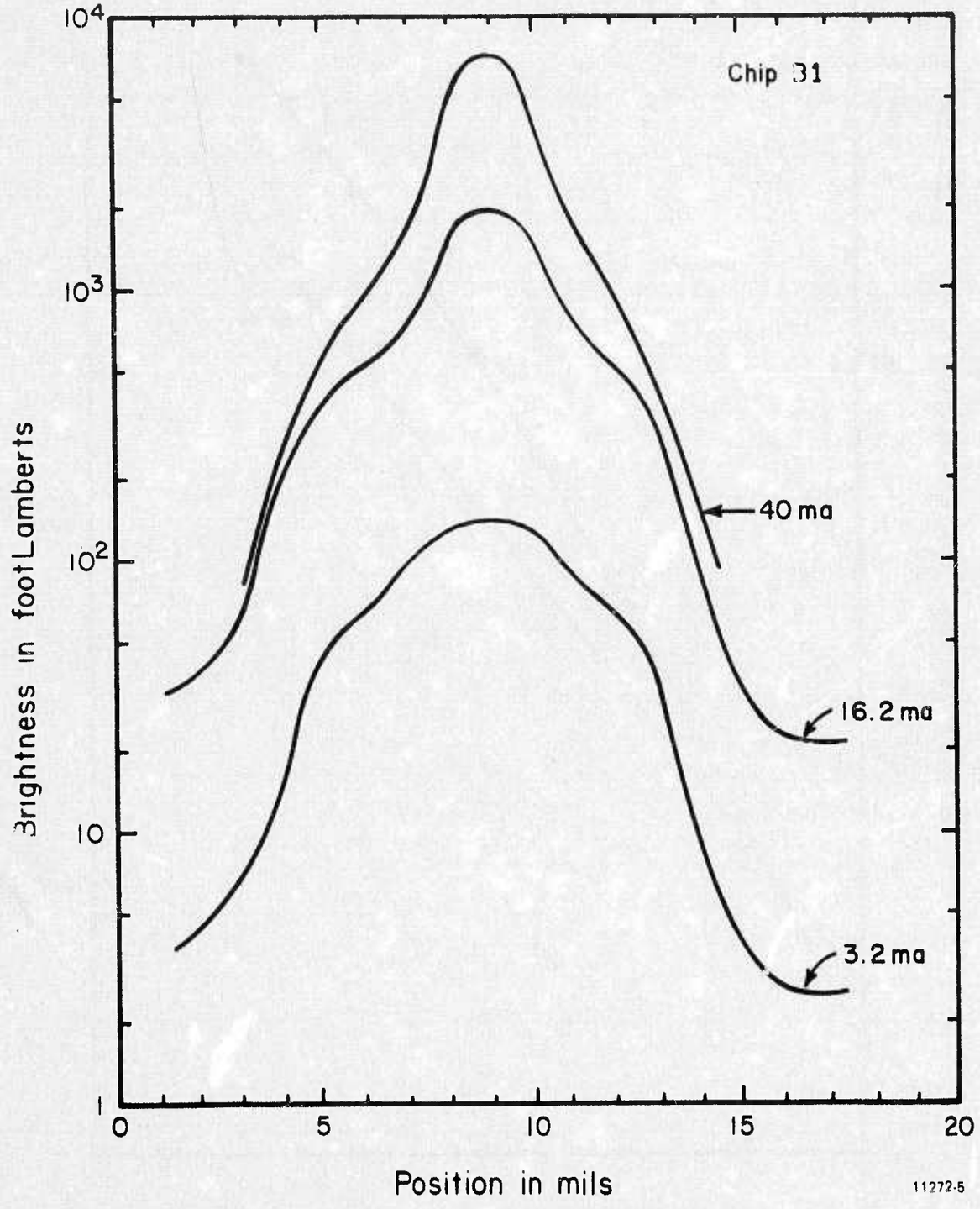


Figure 25. Brightness uniformity across LED junction at various currents.

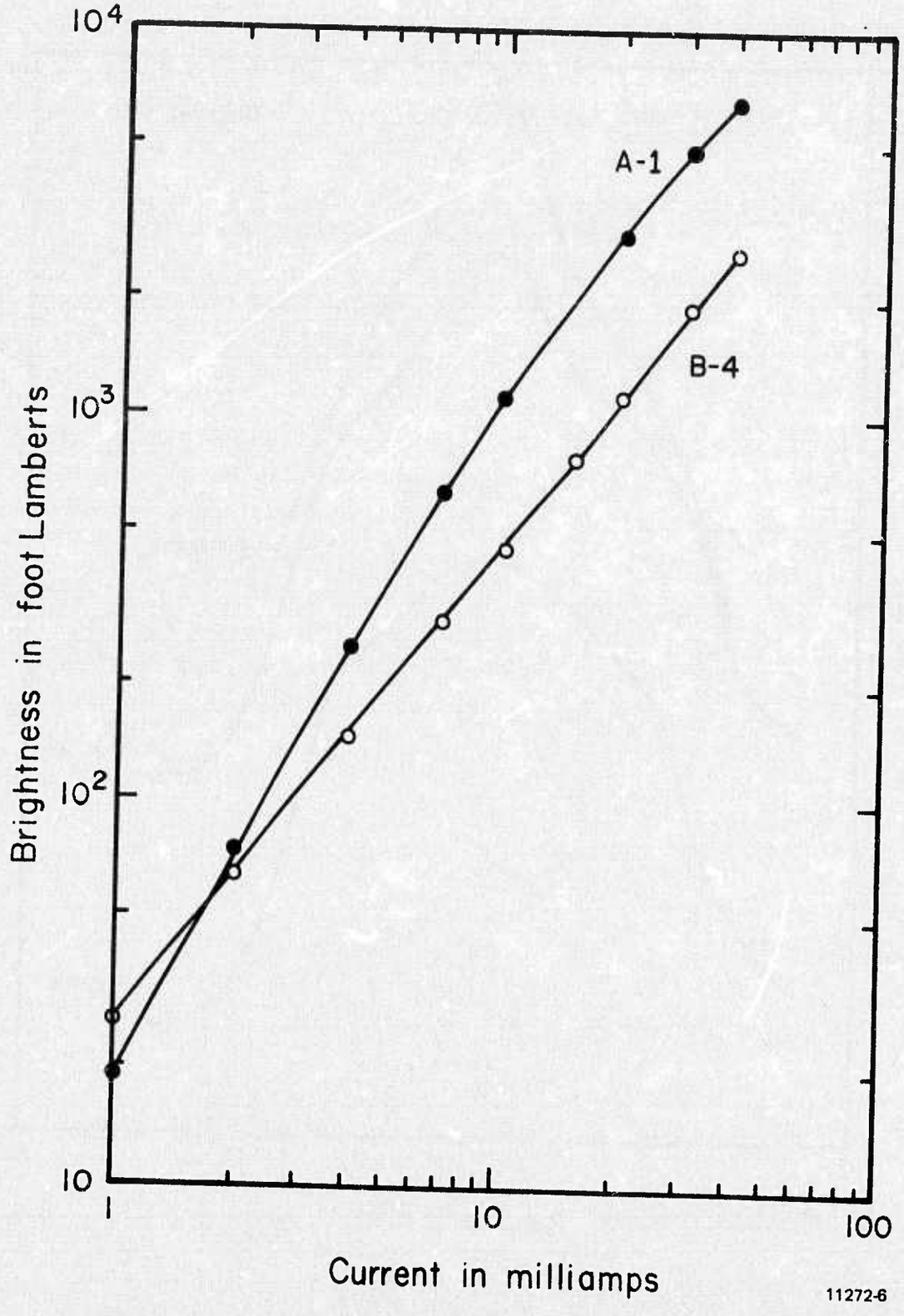
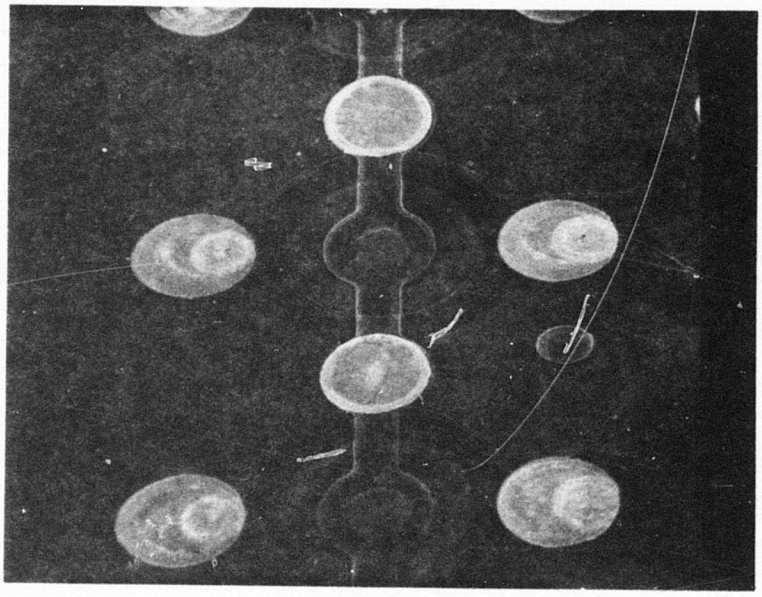


Figure 26. Brightness as a function of forward current.

to 40 ft-L/A/cm^2. The superlinear behavior of the brightness with current makes these devices well suited for multiplexed operation.

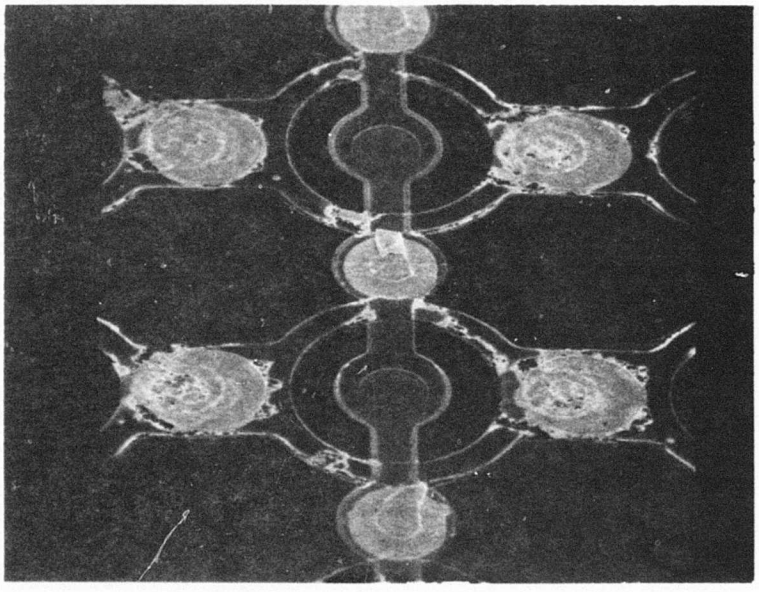
The overall yield obtained in the production of these arrays was very poor. The yield for good wafers (i.e., those providing any good chips) was roughly in the range of 10 to 30 percent. The largest single failure mechanism was shorts in the bilevel metallization patterns. There are many reasons for the poor yields, the most important of which are as follows: (1) the large number of steps involved in processing a single wafer; (2) the existence of 128 crossovers per chip in the bilevel metallization pattern; (3) the lack of match between the thermal expansion coefficient of the glass used and the GaP substrate.

It was not possible to differentiate between good and bad chips on the basis of examination with optical microscopes; however, the scanning electron microscope (SEM) did reveal differences between various chips. Figure 27A shows a SEM picture of a good wafer and Figure 27B shows a bad wafer which exhibited shorts between the bilevel metallization. Figure 28 shows increased magnification of the crossover region of the bad wafer. It is evident that the glass between the n and p interconnect metallization was not impervious to the etchants used on the upper metallization. It is probable that undercutting of the lower metallization prevented a continuous glass cover or that cracks in the glass caused the difficulties in this case.



40240-30

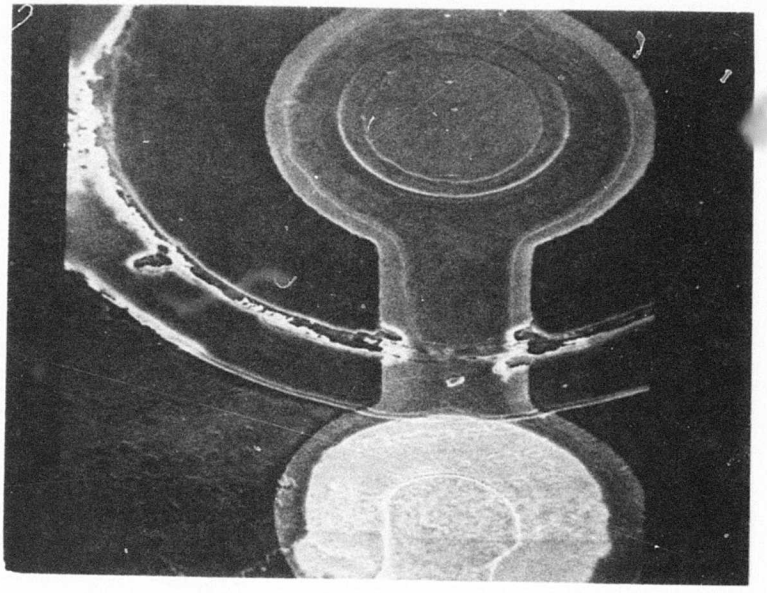
(A) Good wafer.



40240-31

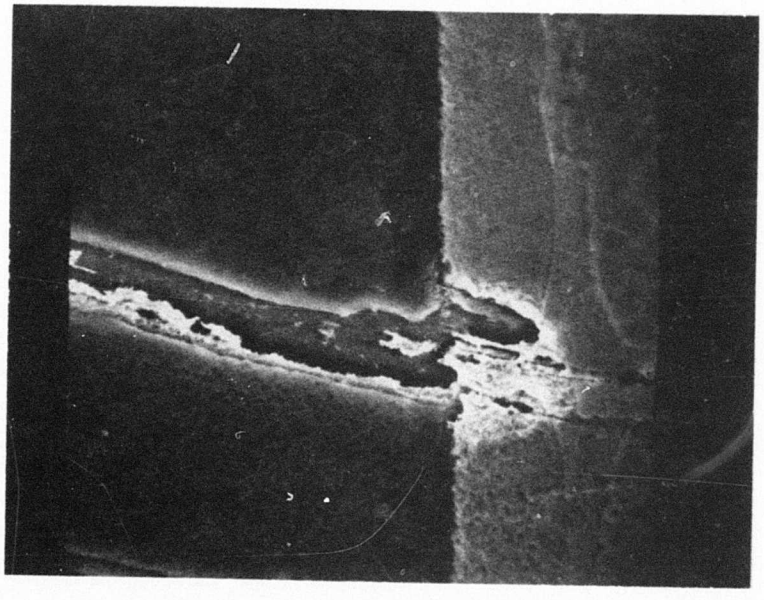
(B) Bad wafer.

Figure 27. SEM photograph of good and bad wafer at 150X magnification.



40240A-32

(A) Bad wafer magnified.



40240A-33

(B) Bad wafer portion further magnified.

Figure 28. SEM photograph of bad wafer.

SECTION 4

CONCLUSIONS AND RECOMMENDATIONS

The Research and Development investigation reported herein has successfully demonstrated the feasibility of utilizing monolithic arrays of LEDs for an aircraft cockpit display. The overall conclusion is drawn after consideration of solutions to the problems that were encountered in obtaining the LED arrays. As noted in Section 3, the overall yield obtained in the production of the arrays was very poor. The yield for good wafers (i.e., those providing any good chips) was roughly in the range of 10 to 30 percent. The largest single failure mechanism was shorts in the bilevel metallization patterns. The reasons for the poor yields are the large number of steps involved in processing a single wafer, the existence of 128 crossovers per chip in the bilevel metallization pattern, and lack of match between the thermal expansion coefficients of the glass used and the GaP substrate. In order for the arrays to be flip-chip bonded, the contacts on the arrays must be solder wettable. Nickel used as the base metal was coated with gold for the solder adherence but the gold did not adhere well to the nickel and the majority of the arrays had 50 percent or more of the gold missing. The nickel formed an oxide where the gold was missing and would not solder. This problem was solved by using conductive epoxy to mount the arrays.

Scanning electronic microscope examinations of shorts between the bilevel metallization showed clearly that the glass between the n and p interconnect metallization was not impervious to the etchants used on the upper metallization. It is probable that undercutting of the lower metallization prevented a continuous glass cover or that cracks in the glass caused the difficulties. The general solution to the production problem then lies in seeking greater imperviousness in the glass.

The problem of metallization crossover shorts was solved by placing a current on the crossover area and burning the short out. In most cases, this technique removed the short without harming the LED. In all cases, removal of the short removed the cross lighted LEDs in the display and cleaned up the surface.

The major problem in the metallization was intermittent opens in the column area, a problem which was not observed until the display surface was assembled. The column metallization is closest to the GaP surface and therefore needed the most build-up to be level with the row bonding pads. Several deposits were needed to build up the column pads and the deposits started separating during display operation to the

point that 35 to 40 of the columns would drop out when a maximum number of LEDs were activated. This was related to the thermal stress in the array; that is, as more LEDs were activated, more power was dissipated in the array and the attendant temperature rise of the array operated the columns pad build-up in the manner of a thermal switch. It is felt that the general solution to this problem is strict adherence to fabrication technique. The optical isolation achieved in the arrays was excellent. Diffusion isolation of the columns was a success as was the number of good LEDs in a chip. Because the problems encountered in development of the monolith LED chips were primarily process problems, they can be solved easily with further development and/or a change in approach to eliminate the metallization crossover. The light output of the LEDs can be increased by incorporation of a drive system that takes advantage of the phenomenom of increased efficiencies at short drive pulses, and also by using LEDs now obtainable that are more efficient than those obtainable two years ago when LEDs for this project were fabricated. Further investigation in the area of monolith structure is recommended to develop a high-yield flip chip that can be bonded to a multilayer, edge joinable substrate, similar to the substrate developed for this program.

Development of the drive system was totally successful, permitting all LEDs on the display to be addressed and scanned by the hybrid drive system mounted on the module. Development of the display generator was also totally successful in that alphanumerics and vectors can be selected and placed at any point in the display surface.

The combined circular-polarizer, spectrum bandpass, and antireflectant front surface filter that was developed to provide contrast enhancement demonstrated a viable approach to the problem of display viewing in an ambient that ranges from 0.01 foot lamberts to 10,000 foot lamberts. Even operating at less than half the LED design brightness, the display is legible under ambient light intensities close to the worst-case condition. The minor degradation experienced with the antireflectant coating on the filter can be corrected by using a standard coating available from Polaroid or OCL. The gel interface in the filter provides a significant gain in apparent brightness and contrast. Consequently, consideration should be given for future applications to constructing these filter assemblies of selected HEA coated neutral circular polarizers and providing the bandpass features by incorporating a suitable transparent dye system (e.g., a dye similar to that used in G.E. 3196 Green Lexan) into the gel interface layer.

The next logical step in the overall program is to develop a full sized (5 inch by 6 inch) prototype display for evaluation. This prototype can take advantage of commercial LED advances in efficiency to obtain an increased light output and be constructed with available technology using three edge-stackable modules. A concurrent program to increase the efficiency of the LEDs and obtain a monolithic flip chip structure is recommended to produce a full edge-joinable module.

APPENDIX A

OPERATING PROCEDURES FOR X-Y GREEN LIGHT EMITTING DIODE (LED) MATRIX MODULE

APPENDIX A

OPERATING PROCEDURES FOR X-Y GREEN LIGHT EMITTING DIODE (LED) MATRIX MODULE

A-1. INTRODUCTION

This appendix describes the functions and operating procedures for the research and development feasibility model X-Y LED Matrix Module, also referred to as the system.

A-2. SYSTEM DESCRIPTION

A-2.1 System Functions

The X-Y LED Matrix Module is a flat panel display composed of green LEDs set in an array 0.75 x 0.50 inch at a resolution of 64 diodes per inch. Its primary function is to display a simulation of an artificial horizon indicator, with aircraft pitch and roll components controlled by a joystick hand control. In addition, alphanumeric characters and vectors can be programmed on the display either manually or by paper tape input.

A-2.2 System Components

The system is constructed in three units as described below and shown in Figure A-1.

a. Display Head - Comprises the display surface itself, along with the immediate diode driver circuits (see Figure A-2).

b. Joystick Head - Contains an X-Y (roll pitch) joystick and reset button (see Figure A-3).

c. Display Control Console - Contains the system power supplies, display processor and manual, and tape interface logic. The display head and joystick head are remoted from the Display Control Console by cables. System power is derived from 115 vac line power, switched at the panel of the Display Control Console.

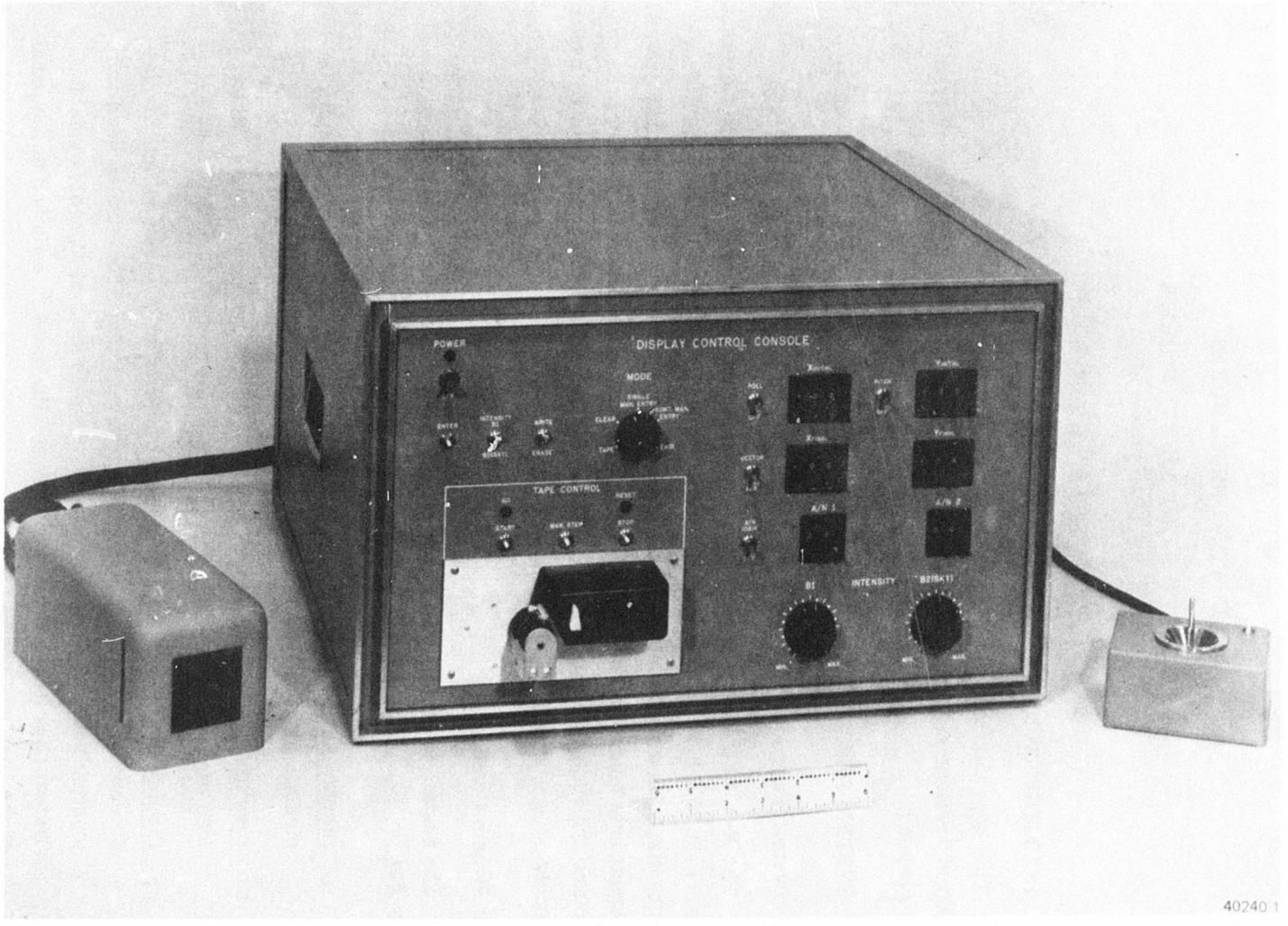


Figure A-1. X-Y LED matrix module.

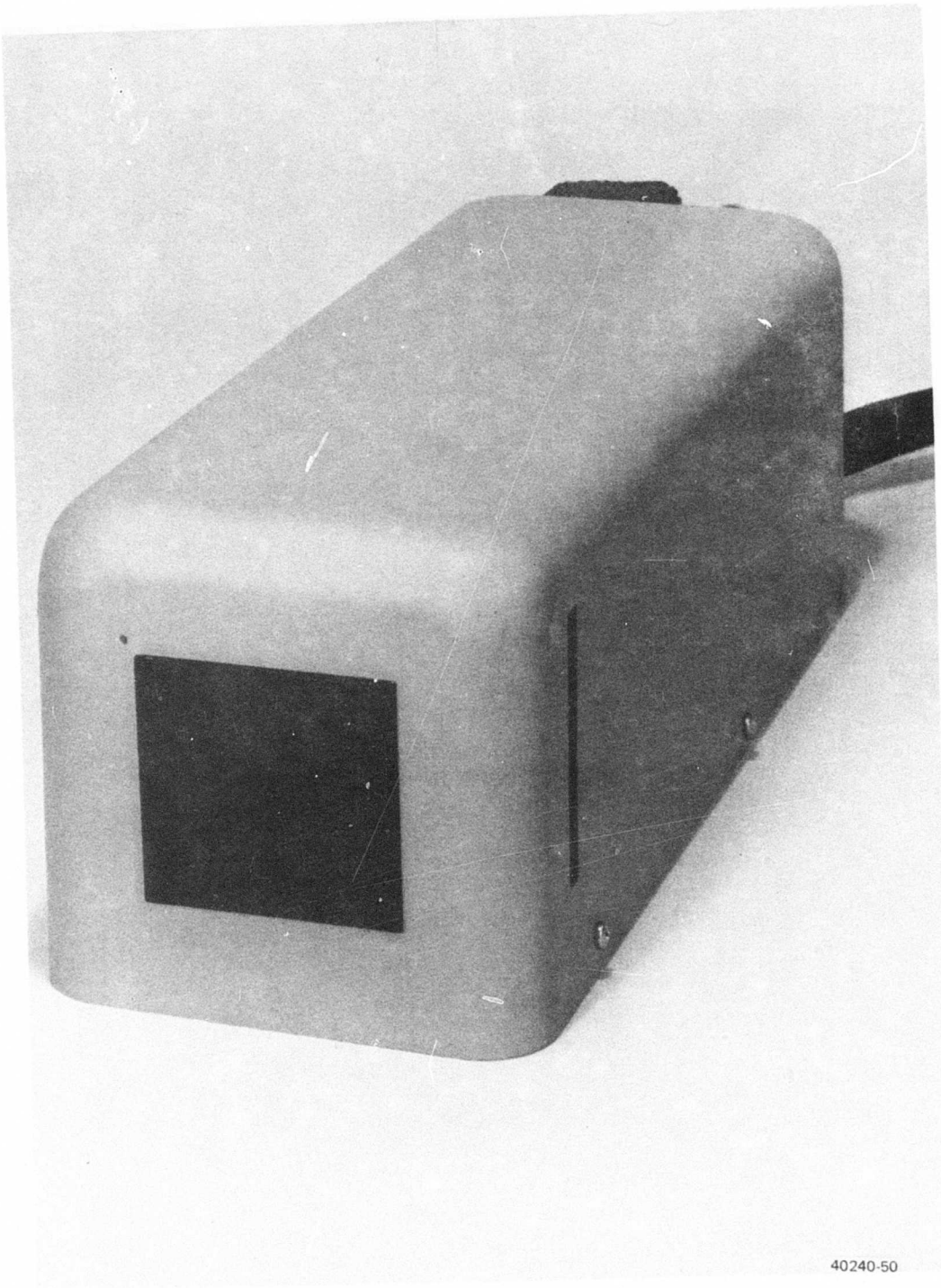


Figure A-2. Display head.

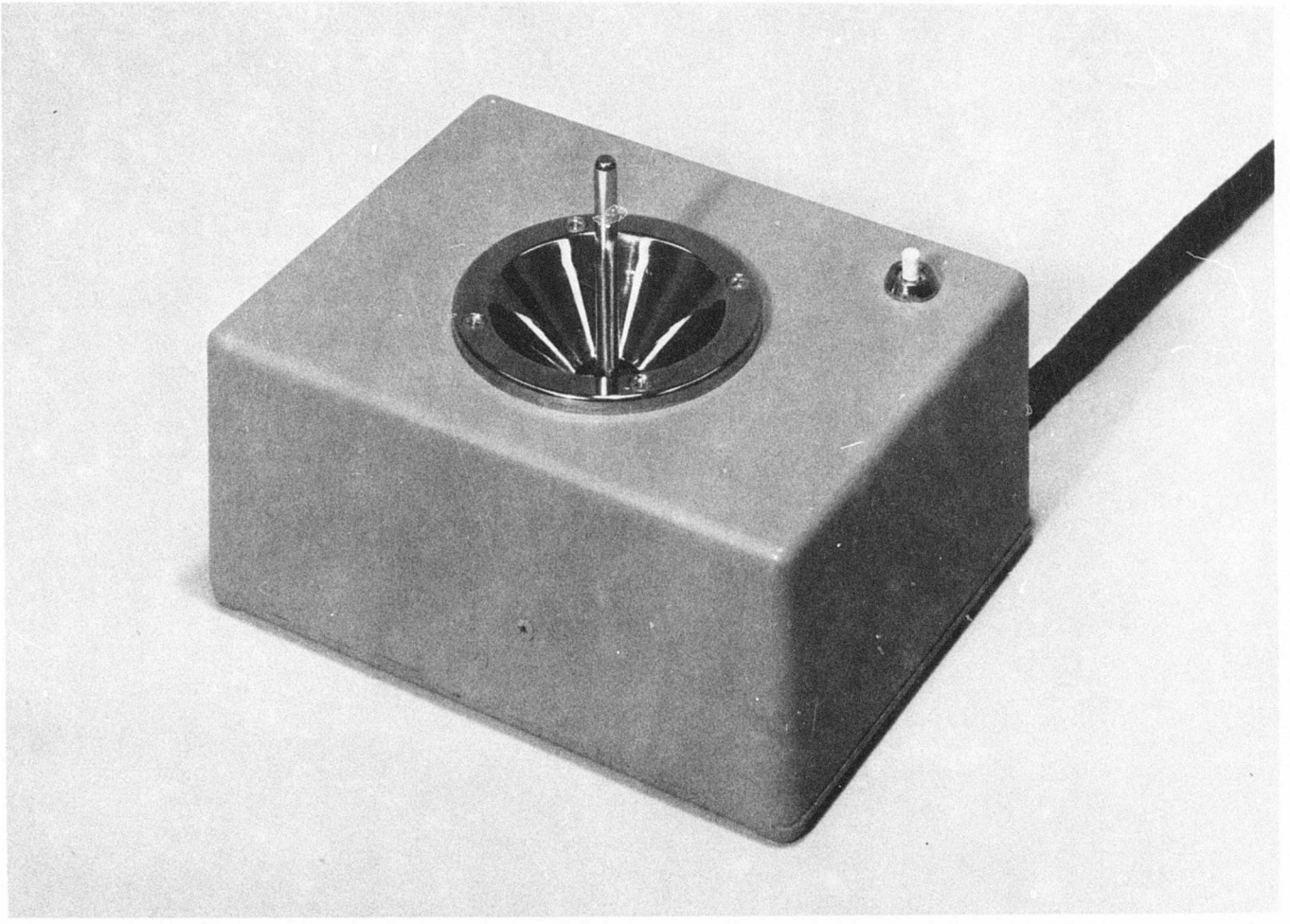


Figure A-3. Joystick head.

A-3. OPERATING PROCEDURE

To identify controls mentioned in this section, refer to Figures A-4, A-5, and A-6.

A-3.1 System Turn-On

Verify that the display head and joystick head are connected via their respective plugs at the rear of the control console. Plug the power cord into a source of 115 vac, 60 Hz power. Turn system power on via the POWER switch located in the upper left corner of the Display Control Console.

A-3.2 EADI Mode

Set switch positions on the Display Control Console as indicated in Table A-1.

TABLE A-1. DISPLAY CONTROL CONSOLE SWITCHES/POSITIONS

Switch	Position
MODE	EADI
ROLL/OFF	OFF
PITCH/OFF	OFF
VECTOR/A/N	VECTOR
X INITIAL	All to +00
Y INITIAL	All to +00
X FINAL	All to +00
Y FINAL	All to +00
B1	Maximum clockwise
B2 (SKY)	See note

NOTE: Reset the roll and pitch registers by means of the button on the joystick head. The display head will now present the artificial horizon display, consisting of a fixed "boresight" pattern and a sky-pitch grid pattern which will move in response to operation of the joystick. The brightness of the boresight and pitch-grid pattern is controlled by INTENSITY switch B1. The brightness of the (SKY) is separately controlled by INTENSITY switch B2.

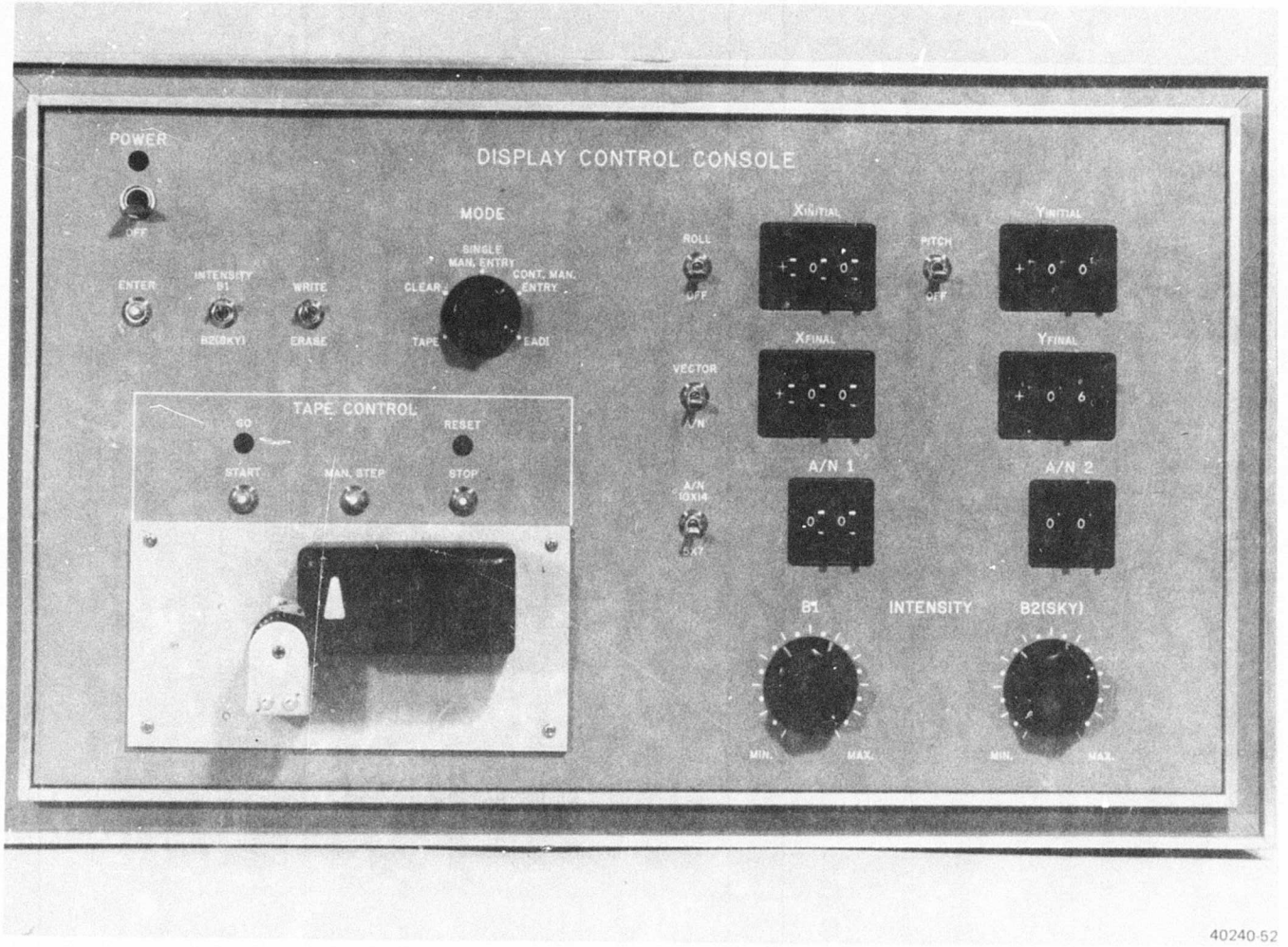


Figure A-4. Display control console-front panel.

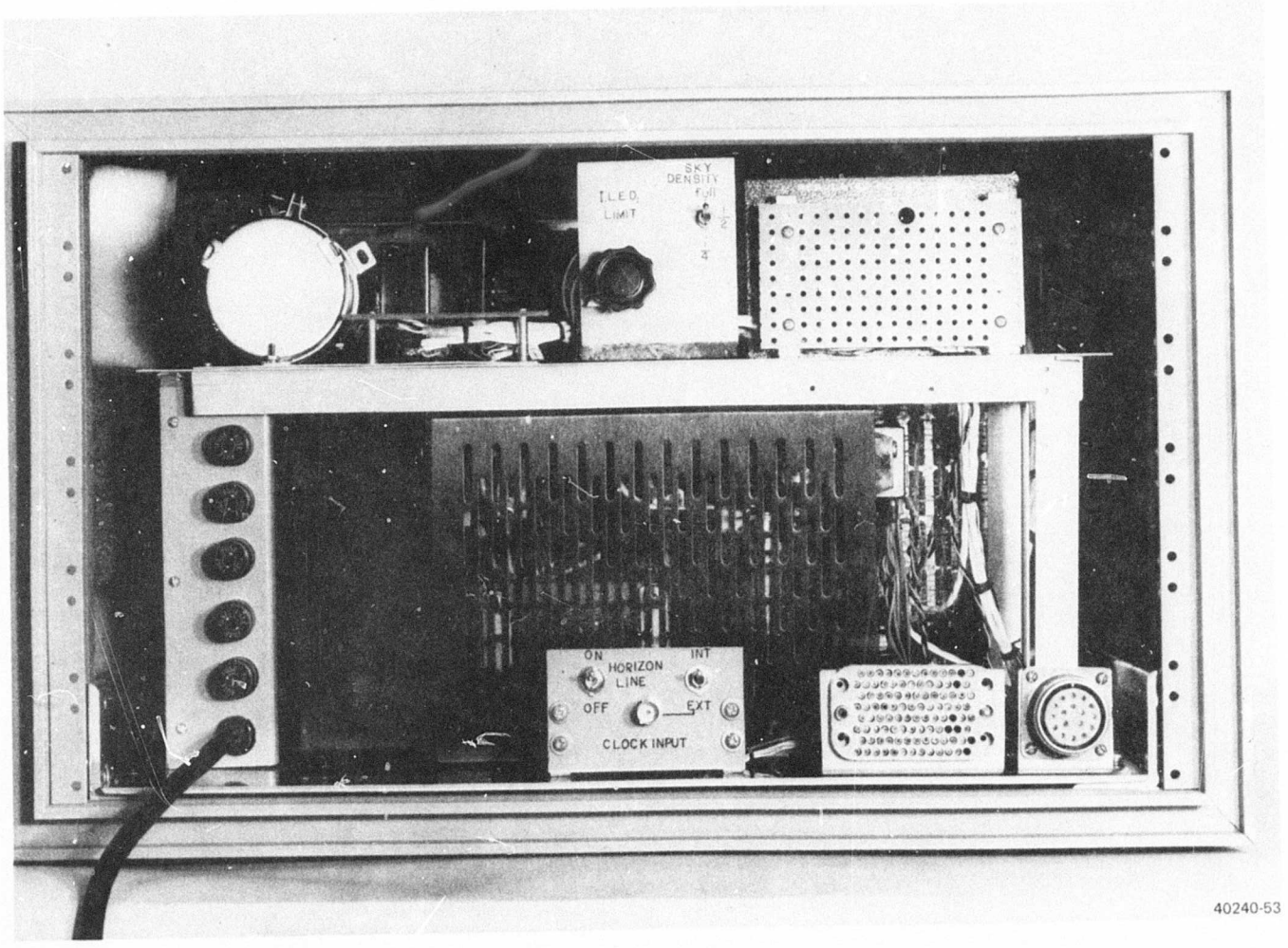


Figure A-5. Display control console-read controls and connectors.

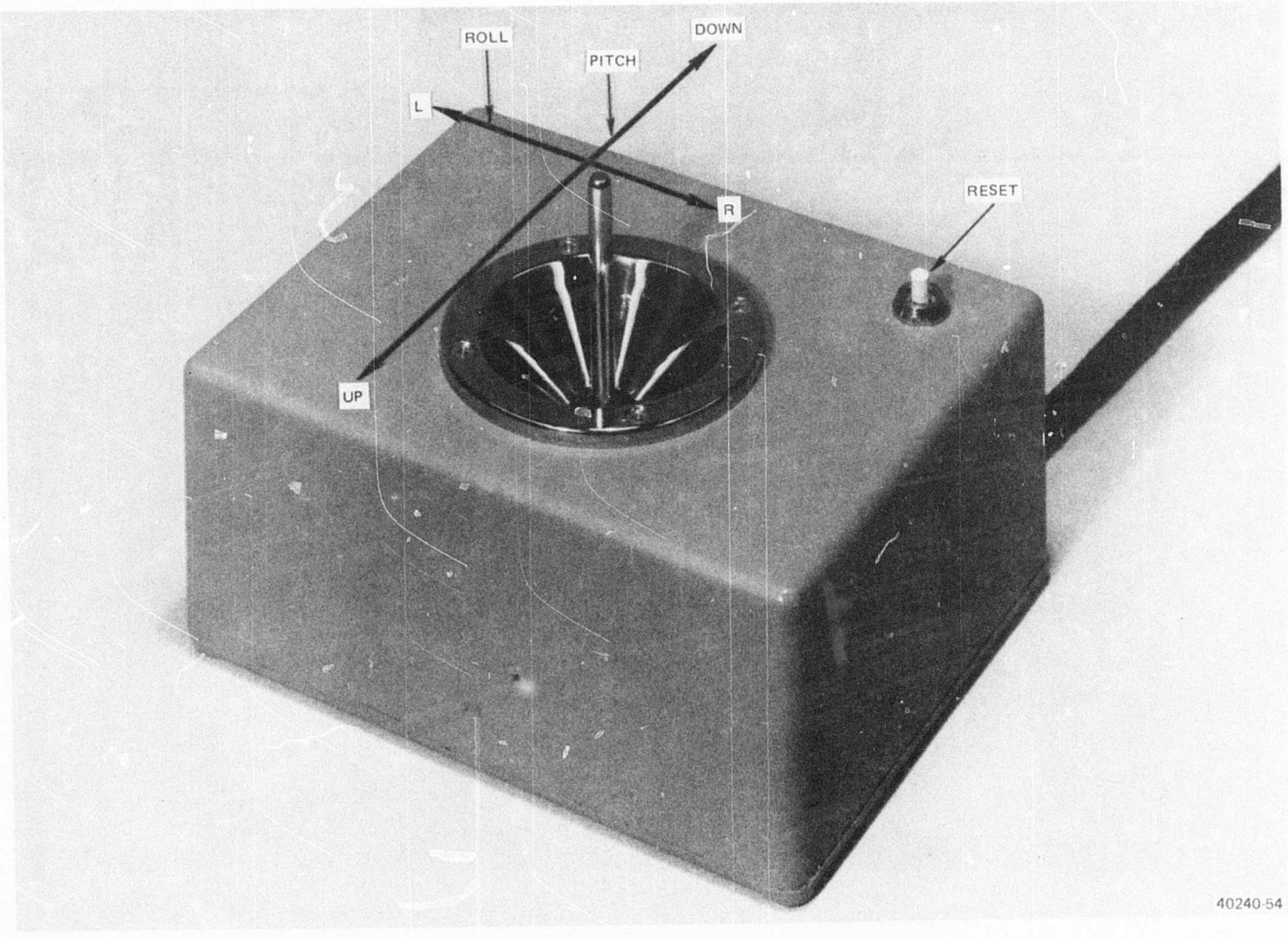


Figure A-6. Joystick configuration.

A-3.3 Manual Entry Mode

The X-Y LED Matrix Module display will display vectors and alphanumerics as commanded by the console switches in two modes, CONT. MAN. ENTRY and SINGLE MAN. ENTRY.

The brightness of entered elements in either mode can be commanded to be controlled by either the INTENSITY B1 or the B2 (SKY) switch by means of the INTENSITY switch near the ENTER button.

A-3.3.1 Continuous Manual Entry - Set the MODE switch to the CONT. MAN. ENTRY position and the WRITE/ERASE switch to WRITE. Figure A-7 shows the Display Coordinate System for the Display Control Console position switches. The X INITIAL/Y INITIAL switches determine the coordinates of the start of a vector or of the lower left corner of an alphanumeric; the X FINAL/Y FINAL switches determine the coordinates of the end of a vector. The VECTOR-A/N switch selects the type of element to be displayed. If the element is A/N, the character to be displayed is selected by the A/N 1 switches per Table A-2.

The A/N - 10 x 14/5 x 7 switch determines the displayed size of the character; the lower left corner remains fixed at the X initial-Y initial coordinates. The A/N 2 switches are not utilized at this time, but provide for future expansion.

The displayed element will respond to the joystick pitch and roll functions if the PITCH and ROLL switches are ON; otherwise, the element coordinates are determined solely by the front panel switches on the Display Control Console. Only a single vector or alphanumeric can be displayed in the Continuous Manual Entry mode.

This mode is also operative when the MODE switch is in the EADI position; the element selected by the panel switches will be displayed in addition to the artificial horizon display.

A-3.3.2 Single Manual Entry - The switches described in the Continuous Manual Entry Mode have the same functions in the Single Manual Entry Mode, with the exception that entry is not automatic. First, the operator sets up the coordinate and element selection switches, then pushes the ENTER button to display the element. (Again, the WRITE/ERASE switch must be in the WRITE position.) This mode operates cumulatively; the coordinate and element selection switches may now be changed and another element entered by again pushing the ENTER button. If the ROLL and PITCH switches are ON, the coordinates of elements entered in this mode will be modified by the roll

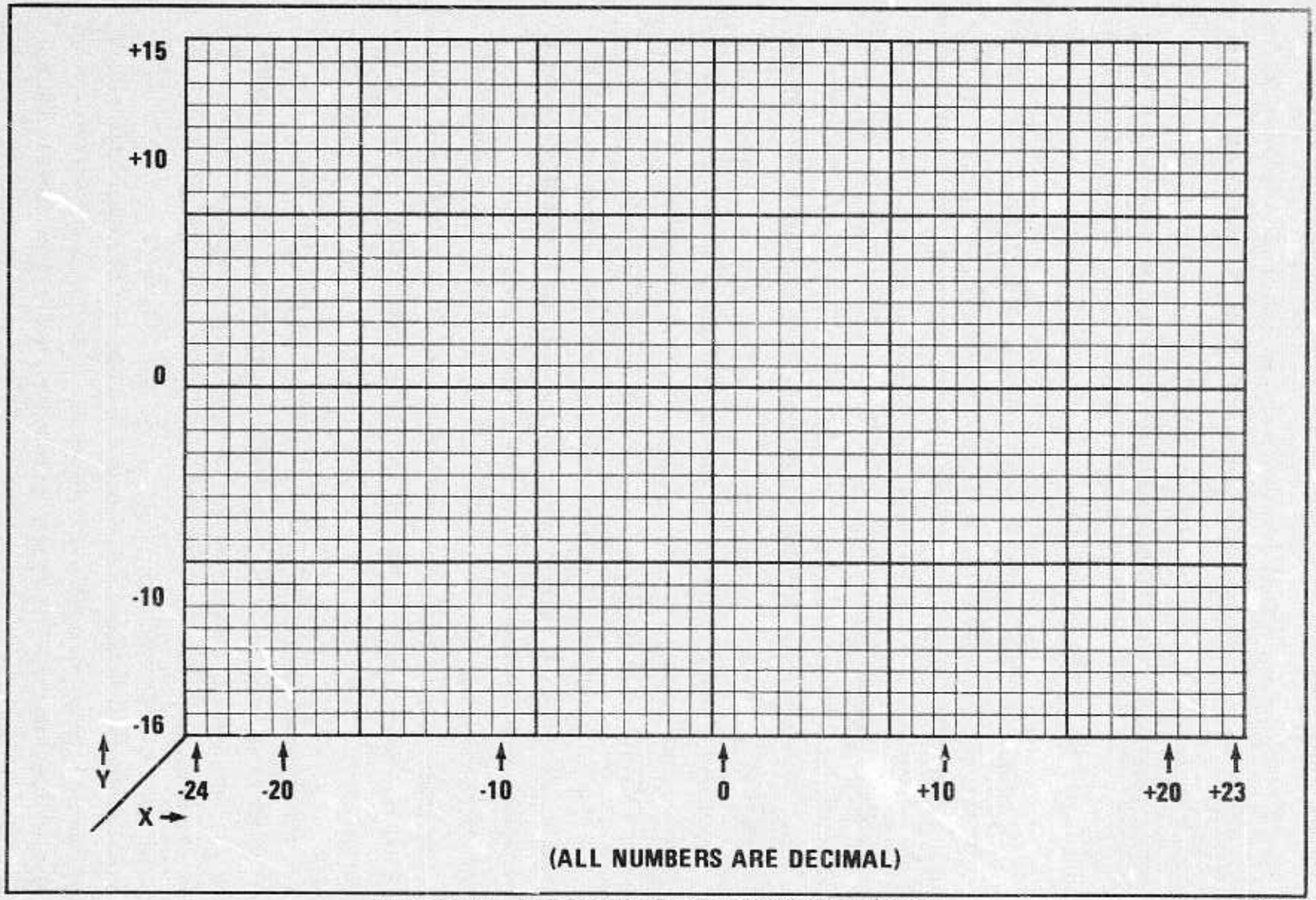


Figure A-7. Display coordinate system manual entry.

40240-55

TABLE A-2. DISPLAY CHARACTER CODES

Character	Code	Character	Code
0	00	I	25
1	01	J	26
2	02	K	27
3	03	L	28
4	04	M	29
5	05	N	30
6	06	O	31
7	07	P	32
8	08	Q	33
9	09	R	34
A	17	S	35
B	18	T	36
C	19	U	37
D	20	V	38
E	21	W	39
F	22	X	40
G	23	Y	41
H	24	Z	42

and pitch values at the time of entry. An element can be selectively erased when the coordinate and element seleetion switches are at the same settings used to enter the element by switching the WRITE/ERASE switch to ERASE and pushing the ENTER button.

A-3.4 Clear Mode

Set the MODE switch to CLEAR. Push the ENTER button and the display will be cleared.

A-3.5 Tape Mode

A-3.5.1 Tape Format - Figure A-8 shows the paper tape byte formats. Each element (a vector or an alphanumeric character) requires a block of paper tape bytes. Each alphanumeric/vector must be separated by an end-of-block (EOB) byte (11111*111).

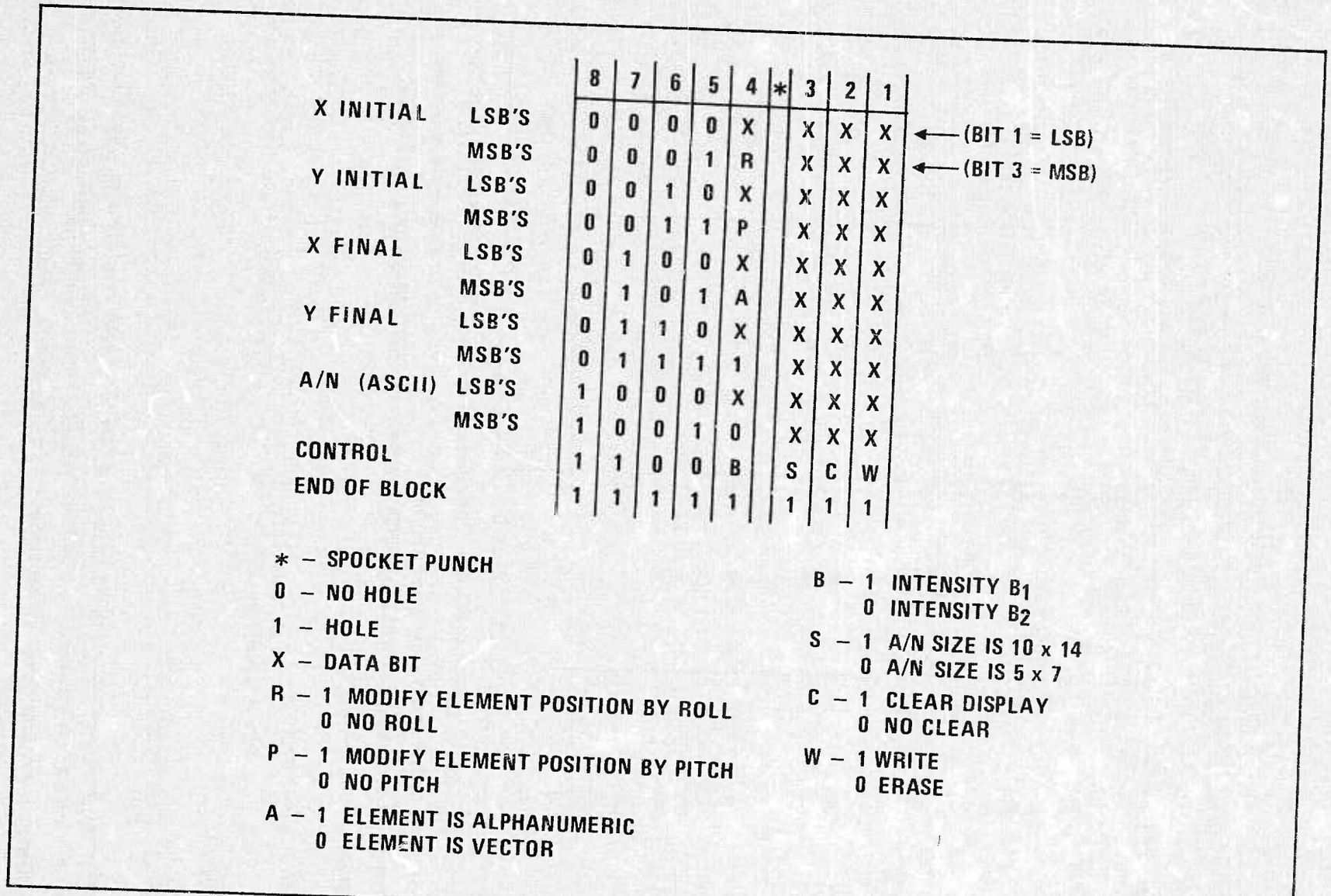


Figure A-8. Tape format.

Bits 5-8 of each byte identify the function of the byte; thus, the least significant bits (LSB) of the X initial position are identified by bits 5-8 being all 0 (not punched). For a vector, nine bytes (not counting the EOB) are required: X initial (LSB), X initial most significant bit (MSB), Y initial (LSB), Y initial (MSB), X final (LSB), X final (MSB) - bit 4 = 0 to specify vector, Y final (LSB), Y final (MSB), and Control. For an alphanumeric, eight bytes (not counting the EOB) are required: X initial (LSB), X initial (MSB), Y initial (LSB), Y initial (MSB), X final (MSB) - bit 4 = 1 to specify alphanumeric, A/N (LSB), A/N (MSB), and Control.

Figure A-9 shows the coordinate system for tape entry. Coordinates are expressed as hexadecimal numbers with negative numbers in 2's complement form:

0 - 0 0 0 0	8 - 1 0 0 0
1 - 0 0 0 1	9 - 1 0 0 1
2 - 0 0 1 0	A - 1 0 1 0
3 - 0 0 1 1	B - 1 0 1 1
4 - 0 1 0 0	C - 1 1 0 0
5 - 0 1 0 1	D - 1 1 0 1
6 - 0 1 1 0	E - 1 1 1 0
7 - 0 1 1 1	F - 1 1 1 1

Alphanumerics are entered in tape format using standard ASCII code.

In Figure A-8, bit 4 of the X initial (MSB) bytes is labelled R. In TAPE MODE, this bit is equivalent to the ROLL switch in SINGLE MAN. ENTRY mode. Similarly, bit 4 of the Y initial (MSB) byte corresponds to the PITCH switch.

The Control byte data bits are labelled B, S, C, and W, with the bits having the following uses: B specifies which intensity control affects the brightness of the element, S specifies the size of an alphanumeric element (no effect on vector), C clears the display (where a control byte with C = 1 can be a block by itself), and W is used to specify the write or erase function.

A-3.5.2 Loading Tape - Set the MODE switch to TAPE. Push the STOP button on the tape reader to reset the system.

Turn the white triangular loading lever so that the triangle points up.

Insert the tape into the reader, meshing the drive sprocket with the sprocket holes in the tape; then rotate the loading lever to the left, engaging the reader star

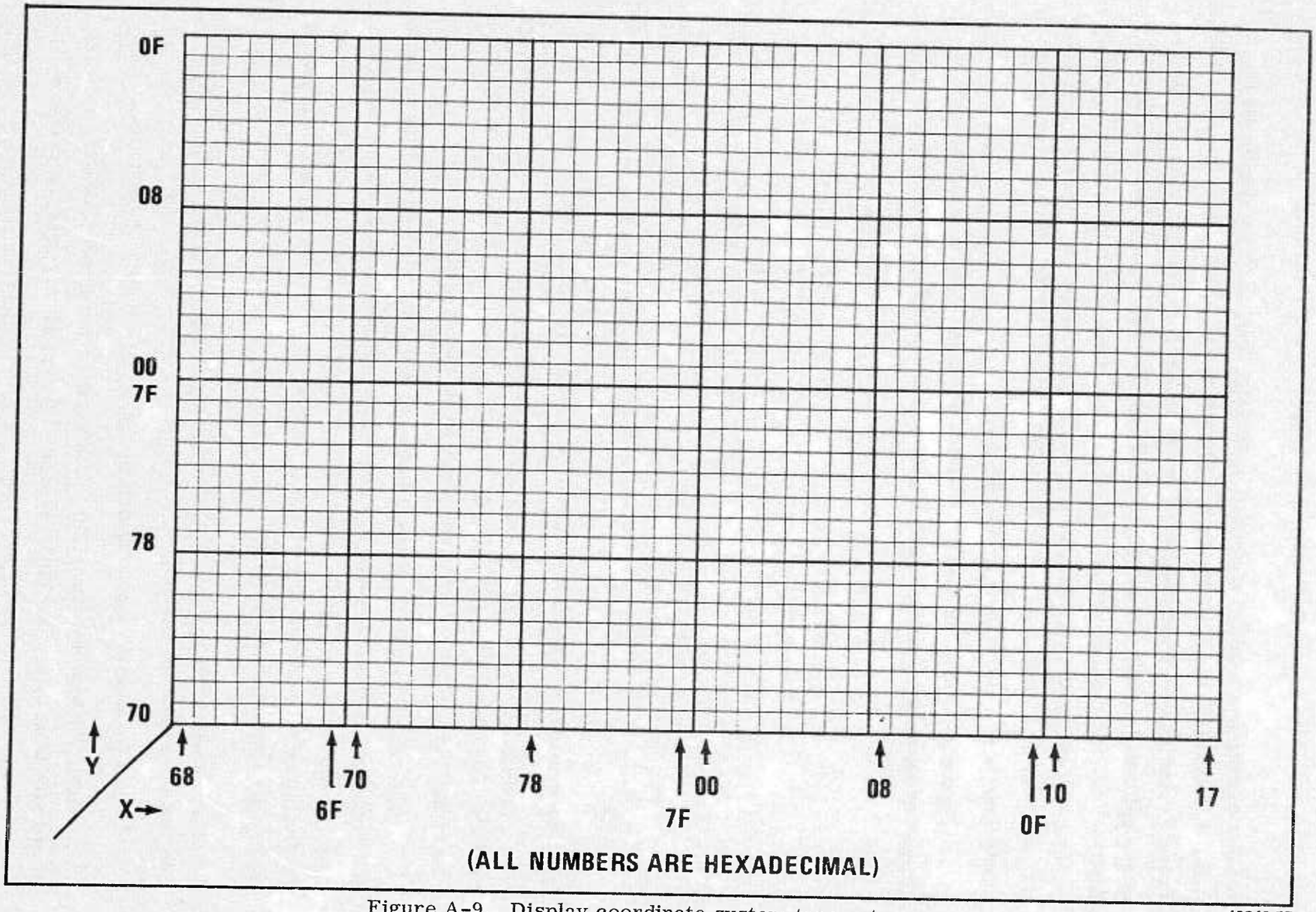


Figure A-9. Display coordinate system tape entry.

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wheels with the tape. Check to see that the tape will not foul as it feeds into the reader. Press the START button, causing the tape to advance through the reader. Each data item will be entered on the display as the EOB character is encountered. The tape may be halted at any time by pressing the STOP button; the reader will stop automatically when the end of the tape is reached (the reader does not reset itself in this condition).

A-3.6 Other Functions

A-3.6.1 System Reset - At any time, the STOP button on the TAPE CONTROL panel will reset the processor and display generator. (The roll and pitch angles are not reset by this button.)

A-3.6.2 Rear Function Switches - Refer to the following subparagraphs for description of the rear function switches and see Figure A-5 for their location.

a. SKY DENSITY Switch - The three-position SKY DENSITY switch allows selection of full density sky (all diodes driven in sky area), one-quarter density sky (every other diode in X and Y), or one-sixteenth density sky (every fourth diode in X and Y). Brightness of the driven diodes is controlled by the B2 (SKY) switch in all three modes.

b. HORIZON LINE Switch - The OFF position of the HORIZON LINE switch suppresses display of the horizon line; the interface between sky and ground continues to respond to the pitch and roll inputs.

c. External Clock Function - A BNC coaxial connector is provided for external clock input, along with a switch for selection of the internal (INT) or external (EXT) clock. The external clock should be a square wave between 0 and 3.5 volts, with rise and fall times less than 50 nanoseconds. The external clock permits observation of phenomena related to the refresh rate of the display generator. Since the processor and the display generator utilize independent clocks, these observations are limited by synchronization timing to static displays produced in the manual or tape entry modes with the internal clock selected. When the desired display is fully loaded, the external clock can be selected and varied in frequency between the limits of 3.2 and 32 MHz. These limits correspond roughly to display refresh rate limits of 100 Hz to 1 kHz.

d. I.L.E.D. LIMIT Control - The I.L.E.D. LIMIT control (located at the top center of the display control console's rear) is used to set the maximum total input current to the LED array and hence limit dissipation in the display head. The approximate limiting currents (and dissipations based on V_{LED} = 8 vdc) are as shown in Table A-3.

TABLE A-3. APPROXIMATE LIMITING CURRENTS

Switch position	Limiting current	Maximum power
1 (full ccw)	200mA	1.6W
2	300mA	2.4W
3	400mA	3.2W
4	540mA	4.3W
5	800mA	6.4W
6	1.2A	9.6W
7	1.4A	11.0W
8	1.7A	13.0W
9	1.8A	14.0W
10	2.4A	19.0W
11	2.8A	22.0W
12 (full cw)	≈7.0A*	≈56.0W*

* Internal supply limiting - varies with temperature.

APPENDIX B

OPERATIONAL PROGRAM FOR DISPLAY PROCESSOR

```
 NAME  AD   OBJECT   AV N AMX Z SKIP SHFT DX MMUX ADMX FLA CRY FLB FWT MASK C DA

MAIN   00 98F7FFFF66 AD N       JMIN      DE                              66
       01 18BFFF1E06 AD         JMIN LREG                        WA1 ZERO  06
       02 7F8EFF0A40 DO                LREG    MDTF                     WA0 BMA0  40
       03 7FBFFF9B7F DO                LREG    MPAN                     WB1 BMA1  7F
       04 7FBFFFAF6F DO                LREG    MPAN                     WB2       6F
       05 18BAFAAB7F AD         JMIN LREG    MFLB               RB2 WB2 BMA1  7F
       06 7FB5F78F21 DO                LREG DE MADD       CR1       WB0       21
       07 7FDEFFFF80 DO                LADD    MDTF                             80
       08 6FB78FBE0F DO   FLA       LREG DE            RA0             WB3 ZERO  0F
       09 6FBF9FCEFF DO   FLA       LREG               RA1             WB4 ZERO
       0A 7F8AFAFFFF DO                LSRA    MFLB               RB2
       0B 7F9EFFFA2D DO                LSRB    MDTF                     BMA0  2D
       0C 67F3F7F73F DO   SRA           DE MSRB       CR1                 C 3F
       0D 7CF7FFFF26 DO         JQMS    DE                               26
       0E FADEFFFF69 DO N       JEAD LADD    MDTF                        69
       0F 7FB87FDF16 DO                LREG    MPRM AMPG           WB5       16
       10 7F82FAFF29 DO                LSRA DE MFLB               RB2       29
       11 197F7FFFFE AD         JSTC SRAK       AMPG                        FE
       12 67C87FFF15 DO   SRA        LSAD    MPRM AMPG                      15
       13 D96F7FFFFF BK N       JSTC SLIN       AMPG                        FF
       14 7FBBFF2FFF DO                LREG    MSRB                WA2
       15 197F7FFFFF AD         JSTC SRAK       AMPG                        FF

       16 67A87FFF12 DO   SRA        LSAM    MPRM AMPG                      12
       17 D97F7FFFFF BK N       JSTC SRAK       AMPG                        FF
       18 7FBBFF3FFF DO                LREG    MSRB                WA3
       19 6FB83F3F17 DO   FLA       LREG    MPRM AMPG RA3           WA3       17
NEXT   1A 6F87AFFE10 DO   FLA       LSRA DE            RA2                ZERO  10
       1B 197F7FFFFE AD         JSTC SRAK       AMPG                        FE
       1C 67C87FFF14 DO   SRA        LSAD    MPRM AMPG                      14
       1D D96F7FFFFF BK N       JSTC SLIN       AMPG                        FF
       1E 67BCFF4FFF DO   SRA       LREG    MSRA                WA4
       1F 7FDEFFFFEC DO                LADD    MDTF                             EC
       20 7FDEFFFF35 DO                LADD    MDTF                             35
       21 4EF827F719 BK   FLA   JZED        MPRM AMPG RA2 CR1                 C 19
HRET   22 6FB84FEF10 DO   FLA       LREG    MPRM AMPG RA4           WB6       10
LOOP   23 7FB8FE0AFF DO                LREG    MPRM AMFB           RB6 WA0 BMA0  FF
       24 7FB8FEFAFF DO                LREG    MPRM AMFB           RB6 WB7 BMA0  FF
       25 6FB9BE1AFF DO   FLA       LREG    MPRS AMFB RA3       RB6 WA1 BMA0  FF
       26 7FBDF78FFF DO                LREG    MADD           CR1      WB0
       27 7FDEFFFF80 DO                LADD    MDTF                             80
       28 6FBF8F5EFF DO   FLA       LREG               RA0             WA5 ZERO
       29 6FBF9F6EFF DO   FLA       LREG               RA1             WA6 ZERO
       2A 7FBAF6EFFF DO                LREG    MFLB           CR1 RB6 WB6
       2B 7FB8FE0AFF DO                LREG    MPRM AMFB           RB6 WA0 BMA0  FF
       2C 6FB9BE1AFF DO   FLA       LREG    MPRS AMFB RA3       RB6 WA1 BMA0  FF
       2D 7FBDF78FFF DO                LREG    MADD           CR1      WB0
       2E 7FDEFFF580 DO                LADD    MDTF                             80
       2F 7FBDF78FFF DO                LREG    MADD           CR1      WB0
       30 7FDEFFFF38 DO                LADD    MDTF                             38
       31 BBF9FEFFFF SK N       JEOQ            MPRS AMFB           RB6
       32 7FDEFFFF49 DO                LADD    MDTF                             49
       33 7FBAF6EFFF DO                LREG    MFLB           CR1 RB6 WB6
       34 7FDEFFFF23 DO                LADD    MDTF                             23
HORIZ  35 7FF7FFFF20 DO                   DE                                    20
       36 7FBEFF4C0A DO                LREG    MDTF                WA4 BM0A  0A
```

```
SEND FP DATA REQUEST TIL DATA NOT RDY.
SET Y (A1) TO 0.   HANG TIL DATA READY.
SET X (A0) TO 1.
COPY PHI FROM FRONT PANEL AND ZERO MSB.
COPY THETA FROM FRONT PANEL.
THETA MSB = 0.  HANG TIL LIST PROC DONE.
SAVE CURRENT ADDRESS + 1.  SET ROLL SW.
BRANCH TO ROLL
SAVE ROLLED X AS COS.  RESET ALL SW.
SAVE ROLLED Y AS SIN
COPY THETA.
COPY X'2D00' (180) TO SRB FROM DATA.
SAVE MSB OF THETA-180
SET SKYUP1 IF 0<THETA<180
BRANCH TO FPGO IF NOT EADI MODE
PICK UP PITCH MAP COUNT FROM PROM (-15)
PUT THETA (B2) IN SRA AND SET ROLL SW.
SHIFT INTO PLACE
     DIVIDE BY 2 (X'80') FROM PROM
     FOR 2 DEGREES PER TICK MARK
SAVE THETAQ.
PUT THETAR IN SRB AND
ZERO SRA THE LONG WAY
     MULTIPLY BY X'0A', 4X NO. OF LEDS
     PER DEGREE TO MOVE BINARY POINT.
SAVE MODIFIED THETAR.
ADD 35 (X'2300') TO OFFSET THETAR.
PUT THETAQ IN SRA.  ZERO HORIZON SW
SHIFT INTO PLACE
     DIVIDE BY X'05' FOR 5
     KINDS OF TICK MARKS.
DOUBLE AND SAVE REMAINDER (LR) IN TEMP.
BRANCH TO PATCH2
BRANCH TO HORIZ.
GO BACK IF THETAQ-97 IS ZERO.
ADD PROM ADDRESS OF PITCH MAP.
GET X FROM PROM (INDEXED BY LR).
SAVE X FOR LATER USE.
GET Y FROM PROM (LR), ADD THETAR.
SAVE CURRENT ADDRESS+1.
BRANCH TO ROLL.
SAVE ROLLED X.
SAVE ROLLED Y.
INCREMENT LR.
GET X FROM PROM (INDEXED BY LR).
GET Y FROM PROM (LR), ADD THETAR.
SAVE CURRENT ADDRESS + 1.
BRANCH TO ROLL.
SAVE CURRENT ADDRESS + 1.
BRANCH TO HORIZ2.
SKIP IF NOT EOS
BRANCH TO MORE.
INCREMENT LR.
BRANCH TO LOOP.
SET HORIZON SENSE SWITCH.
SET LR = 10.
```

```
 NAME  AD   OBJECT    AV N AMX Z SKIP SHFT DX MMUX ADMX FLA CRY FLB FWT MASK C DA
       37 7FDEFFFF22 DO                LADD    MDTF                          22
HORIZ2 3B 2B9FDFFEF0 SK   FLA   JMIN LSRB                RA5                F0
       39 7FDEFFFFAB DO                LADD    MDTF                          A8
       3A 7F8AFAFFFF DO                LSRA    MFLB            RB2           
       3B 23FEF7F716 SK   SRA   JCAR            MDTF        CR1           C 16
       3C 7FDEFFFF42 DO                LADD    MDTF                          42
       3D 45FEF7F744 BK   SRA   JCAR            MDTF        CR1           C 44
       3E 2EF387F726 SK   FLA   JZED       DE   MSRB        RA0 CR1       C 26
       3F BEFAFBFAB0 SK N       JZED            MFLB            RB3     BMA0  80
       40 7FF7FFFF16 DO                    DE                                16
       41 7FDEFFFFA8 DO                LADD    MDTF                          A8
HOR    42 2EF387F716 SK   FLA   JZED       DE   MSRB        RA0 CR1       C 16
       43 BEFAFBFA80 SK N       JZED            MFLB            RB3     BMA0  80
       44 7FF7FFFF26 DO                    DE                                26
       45 7FDEFFFFA8 DO                LADD    MDTF                          A8
       46 7FDEFFFF1A DO                LADD    MDTF                          1A
       47 4FB837371A BK   FLA           LREG    MPRM AMPG RA3 CR1     WA3   C 1A
       4B 4FBFA72EFF BK   FLA           LREG                RA2 CR1   WA2 ZERO
MORE   49 DEB2F5DF10 BK N       JZED LREG DE MFLB            CR1 RB5 WB5       10
       4A 7FB07FDF11 DO                LREG DE MPRM AMPG                 WB5   11
SMORE  4B BBB8FD0AFF SK N       JEOQ LREG    MPRM AMFB          RB5 WA0 BMA0
       4C 6FB7BFFE21 DO   FLA       LREG DE                RA0           WB7 ZERO  21
       4D BBB9FD1AFF SK N       JEOQ LREG    MPRS AMFB          RB5 WA1 BMA0
       4E 7FDEFFFF51 DO                LADD    MDTF                          51
NPITCH 4F 7FBFFF3EFF DO                LREG                              WA3 ZERO
       50 7FDEFFFF5D DO                LADD    MDTF                          5D
PITCH  51 7FBAFA3FFF DO                LREG    MFLB            RB2 WA3
       52 2DFEBFFAFD SK   FLA   JCAR            MDTF        RA3           BMA0  FD
       53 7FDEFFFF57 DO                LADD    MDTF                          57
       54 2DFEBFFAA9 SK   FLA   JCAR            MDTF        RA3           BMA0  A9
       55 7FDEFFFF7A DO                LADD    MDTF                          7A
       56 6FBEBF3AA6 DO   FLA           LREG    MDTF        RA3           WA3 BMA0  A6
PIT    57 6F9FBFFEFF DO   FLA           LSRB                RA3           ZERO
       58 7FBFFFFEFF DO                LSRA                              ZERO
       59 67A87FFF13 DO   SRA           LSAM    MPRM AMPG                         13
       5A D97F7FFFFF BK N       JSTC SRAK            AMPG                      FF
       5B 7FBBFF3FFF DO                LREG    MSRB                          WA3
       5C 6FBB9F1FFF DO   FLA           LREG    MSRB        RA1               WA1
PITCHD 5D 7FBDF78FFF DO                LREG    MADD            CR1           WB0
       5E 7FDEFFFFB0 DO                LADD    MDTF                          80
       5F 6FB7BF5E13 DO   FLA           LREG DE                RA0           WA5 ZERO  13
       60 ABBF9F6EF2 SK N FLA   JMIN LREG                      RA1           WA6 ZERO  F2
       61 7FDEFFFF6F DO                LADD    MDTF                          6F
       62 7FBAF5DFFF DO                LREG    MFLB            CR1 RB5 WB5
       63 6FB9BD1AFF DO   FLA           LREG    MPRS AMFB RA3     RB5 WA1 BMA0
       64 BBB8FD0AFF SK N       JEOQ LREG    MPRM AMFB          RB5 WA0 BMA0
       65 7FDEFFFF73 DO                LADD    MDTF                          73
PITCH2 66 7FBDF7BFFF DO                LREG    MADD            CR1           WB0
       67 7FDEFFFFB0 DO                LADD    MDTF                          80
       68 7FDEFFFF77 DO                LADD    MDTF                          77
FPGO   69 7FF7FFFF22 DO                    DE                                22
       6A BBBFFF0F0F SK N       JEOQ LREG    MPAN                          WA0   0F
       6B 6FB7BFFE21 DO   FLA       LREG DE                RA0           WB7 ZERO  21
       6C 3BBFFF1F1F SK         JEOQ LREG    MPAN                          WA1   1F
       6D 7FDEFFFF4F DO                LADD    MDTF                          4F
```

```
       BRANCH TO HRET.
       PUT XI IN SRB.  SKIP IF HORIZ SW SET.
       BRANCH TO PAINT
       PUT THETA IN SRA.
       SKIP IF THETA > 88.
       BRANCH TO HOR
       BACK UP IF THETA > 272.
       SKIP IF XI = XF.  SET SKYUP SWITCH.
       SKIP IF COS < 0.
       RESET SKYUP SWITCH.
       BRANCH TO PAINT
       SKIP IF XI = XF.  RESET SKYUP SWITCH.
       SKIP IF COS < 0.
       SET SKYUP SWITCH.
       BRANCH TO PAINT.
       BRANCH TO NEXT.
       SUB 5 FROM THETAR MS BYTE.  (BACK UP).
       ADD 1 TO THETAQ.  (BACK UP).
       INC.  COUNT (BACK IF <0); ZERO HOR.  SW.
       PICK UP ADDRESS OF EADI FROM PROM &
       RESET ROLL SWITCH
       GET X (PROM) AND SKIP IF NOT ROLL.
       SET ROLL SENSE SWITCH.  SAVE INITIAL X.
       GET Y (PROM), SKIP IF NOT PITCH.
       BRANCH TO PITCH.
       SET THETA = 0.
       BRANCH TO PITCHD.
       COPY THETA.
       SKIP IF THETA > 12.
       BRANCH TO PIT.
       SKIP IF THETA > 348.
       BRANCH TO EOSCHK.
       ADD OFFSET TO THETA TO MAKE IT NEG.
       PUT THETA IN SRB.
       ZERO SRA.
            MULTIPLY BY X'0A', 4X NO.  OF LEDS
            PER DEGREE TO MOVE BINARY POINT.
       PUT MODIFIED THETA BACK IN REG FILE A.
       ADD THETA TO Y.
       SAVE CURRENT ADDRESS + 1.
       BRANCH TO ROLL.
       SAVE INIT.  ROLLED X.  RESET LINE SWITCH
       SAVE INITIAL ROLLED Y.  SKIP IF EADI.
       BRANCH TO FPEND.
       INCREMENT COUNT BY ONE.
       READ Y FROM PROM(COUNT) AND ADD THETA.
       READ X FROM PROM.  SKIP IF NOT ALPHA.
       BRANCH TO ALPHA.
       SAVE CURRENT ADDRESS +1.
       BRANCH TO ROLL.
       BRANCH TO PAINTR
       SET "NOT EADI" SWITCH.
       GET X FROM FRONT PANEL.  SKIP NOT ROLL
       SET ROLL SENSE SWITCH.  SAVE INITIAL X.
       GET Y FROM FRONT PANEL.  SKIP IF PITCH.
       BRANCH TO NPITCH.
```

```
 NAME  AD   OBJECT   AV N AMX Z SKIP SHFT DX MMUX ADMX FLA CRY FLB FWT MASK C DA

      6E 7FDEFFFF51 DO                LADD    MDTF                                51
FPEND 6F 6FBFBF1F3F DO    FLA       LREG    MPAN       RA3          WA1         3F
      70 3B8FFF0F2F SK          JEOQ LREG    MPAN                    WA0         2F
      71 7FDEFFFF66 DO               LADD    MDTF                                66
      72 7FDEFFFF75 DO               LADD    MDTF                                75
ALPHA 73 7FBFFF0F5F DO               LREG    MPAN                    WA0         5F
      74 3BF9FDFFFF SK          JEOQ         MPRS AMFB          RB5
ALPHA2 75 7FBFFF0F4F DO              LREG    MPAN                    WA0         4F
      76 7FF7FFFF23 DO                  DE                                      23
PAINTR 77 7FBDF78FFF DO              LREG    MADD          CR1       WB0
      78 7FDEFFFFA8 DO               LADD    MDTF                                A8
      79 3FF7FFFF11 SK                  DE                                      11
EOSCHK 7A 7FB2F5DF11 DO              LREG DE MFLB          CR1 RB5 WB5           11
      7B 7BD7FFFEF2 DO          JMIN LADD DE                          ZERO      F2
      7C BBF9FDFFFF SK N        JEOQ         MPRS AMFB          RB5
      7D 7FDEFFFF69 DO               LADD    MDTF                                69
      7E 7FBAF5DFFF DO               LREG    MFLB          CR1 RB5 WB5
      7F 7FDEFFFF4B DO               LADD    MDTF                                4B
KOLL  80 38BAF9FFF1 SK          JMIN LSRA    MFLB                RB1             F1
      81 7FDAF0FFFF DO               LADD    MFLB          CR1 RB0
      82 190F7FFFF0 AD          JSTC SLLG         AMPG                          F0
      83 67BEF7425A DO    SRA       LREG    MDTF          CR1       WA4 BMA0 C 5A
      84 7FBAFE7FFF DO               LREG    MFLB                RB6 WA7
      85 7FBEF7E402 DO               LREG    MDTF          CR1       WB6 BM0A C 02
      86 6F9F8FFEFF DO    FLA       LSR8                RA0                 ZERO
      87 7F8BF7F7FF DO               LSRA    MSRB          CR1                   C
      88 6F9F9FFEFF DO    FLA       LSRB                RA1                 ZERO
      89 7F9BF7F7FF DO               LSRB    MSRB          CR1                   C
      8A 7FBFFF0EFF DO               LREG                                WA0 ZERO
      8B 7F8FFF1EFF DO               LREG                                WA1 ZERO
KOLL2 8C 6FF7CFFE3F DO    FLA           DE                RA4                 ZERO  3F
      8D 6CBC9717FF DO    FLA   JQMS LREG    MSRA        RA1 CR1       WA1         C
      8E ECBC9F1FFF DO N FLA    JQMS LREG    MSRA        RA1           WA1
      8F ECEB8707FF DO N FLA    JQMS LSAG    MSRB        RA0 CR1       WA0         C
      90 6CED8F0FFF DO    FLA   JQMS LSAG    MSRB        RA0           WA0
      91 AB989EFEFF SK N FLA    JEOQ LSRB    MPRM AMFB   RA1     RB6       ZERO
      92 7FDEFFFF99 DO               LADD    MDTF                                99
      93 ECB8C647FF DO N FLA    JQMS LREG    MPRM AMFB   RA4 CR1 RB6 WA4         C
      94 6CB8CE4FFF DO    FLA   JQMS LREG    MPRM AMFB   RA4     RB6 WA4
      95 7FB2F6EF3F DO               LREG DE MFLB              CR1 RB6 WB6         3F
      96 3CFFFFFFFF SK          JQMS
      97 193FFEFFFF AD          JSTC SRAR         AMFB                RB6
      98 7FDEFFFF8C DO               LADD    MDTF                                8C
REOS  99 7F9FFFFEFF DO               LSRA                                ZERO
      9A 67A87FFF0F DO    SRA       LSAM    MPRM AMPG
      9B D97F7FFFFF BK N        JSTC SRAK         AMPG                          0F
      9C 194F7FFFF1 AD          JSTC SLGK         AMPG                          FF
      9D 7FBCFF1FFF DO               LREG    MSRA                WA1           F1
      9E 7F8FFFFEFF DO               LSRA
      9F 6F9F8FFEFF DO    FLA       LSRB                RA0                 ZERO
      A0 67A87FFF0F DO    SRA       LSAM    MPRM AMPG                       ZERO
      A1 D97F7FFFFF BK N        JSTC SRAK         AMPG                          0F
      A2 194F7FFFF1 AD          JSTC SLGK         AMPG                          FF
      A3 7FBCFF0FFF DO               LREG    MSRA                WA0           F1
      A4 6FBFFFEEFF DO    FLA       LREG                RA7           WB6 ZERO
      A5 7FDAF0FFFF DO               LADD    MFLB              CR1 RB0
```

```
BRANCH TO PITCH.
GET Y FROM FRONT PANEL AND ADD THETA.
GET X FROM FRONT PANEL.  SKIP IF ALPHA
BRANCH TO PITCH2.
BRANCH TO ALPHA2.
PUT ASCII 2 FROM F.P.  INTO X REG.
SKIP IF END OF SEQUENCE.
PUT ASCII 1 FROM F.P.  INTO X REGISTER.
SET LINE SWITCH
SAVE CURRENT ADDRESS + 1.
BRANCH TO PAINT.
RESET ROLL SWITCH AND SKIP.
INCREMENT COUNT AND RESET ROLL SWITCH.
IF NOT EADI MODE, PROC LIST & GO TO 0.
SKIP IF NOT END OF SEQUENCE.
BRANCH TO FPGO.
INCREMENT COUNT BY ONE.
BRANCH TO SMORE.
PICK UP PHI.  SKIP IF ROLL SET.
RETURN TO CALLING PROGRAM.
SHIFT LEFT ONCE.
SUBTRACT 180 FROM PHI.
SAVE LR.
SET INDEX TO MINUS TWO.
COPY X.
INVERT X.  PUT IN SRA.
COPY Y.
INVERT Y.  PUT IN SRB.
ZERO X.
ZERO Y.
SET QMSB WITH SIGN BIT OF PHI.
SUB SRA FROM Y TO FIND NEW Y IF PHI<0.
ADD  SRA TO Y TO FIND NEW Y IF PHI>0.
SUB SRB FROM X TO FIND NEW X IF PHI>0.
ADD SRB TO X TO FIND NEW X IF PHI<0.
PUT Y IN SRB.  SKIP IF EOS BIT NOT SET.
BRANCH TO REOS.
SUBTRACT INCREMENT FROM PHI IF PHI>0.
ADD INCREMENT TO PHI IF PHI<0.
INCREMENT INDEX AND SAVE QMSB.
SKIP IF INDEX < 0.
SHIFT SRA & SRB RIGHT (INDEX+1) TIMES.
BRANCH TO ROLL2.
ZERO SHIFT REGISTER A.
     MULTIPLY Y BY
     CORDIC CONSTANT.
SHIFT LEFT TWICE TO JUSTIFY BINARY PT.
SAVE Y.
ZERO SHIFT REGISTER A.
PUT X INTO SRB.
     MULTIPLY X BY
     CORDIC CONSTANT.
SHIFT LEFT TWICE TO JUSTIFY BINARY PT.
SAVE X.
RESTORE LR.
RETURN TO CALLING PROGRAM.
```

```
NAME   AD  OBJECT       AV N AMX Z SKIP SHFT DX MMUX ADMX FLA CRY FLB FWT MASK C DA

PAINT  A8 A88FDFFEF3  SK N FLA    JMIN LSRA                RA5              ZERO   F3   PUT START X IN SRA.  SKIP IF NOT ALPHA.
       A9 7FDEFFFFE6  DO               LADD    MDTF                                E6   BRANCH TO PALPH.
       AA 6F97EFFE25  DO   FLA         LSRB DE             RA6              ZERO   25   PUT START Y IN SRB.  SET TAN SW.
       AB 6FF487F73F  DO   FLA              DE MSRA        RA0 CR1               C 3F   SAVE MSB OF XF-XI.
       AC 6CBF8F5EFF  DO   FLA    JQMS LREG                RA0         WA5 ZERO         COPY FINAL X TO INITIAL X IF DX < 0.
       AD 6CBF9F6EFF  DO   FLA    JQMS LREG                RA1         WA6 ZERO         COPY FINAL Y TO INITIAL Y IF DX < 0.
       AE 7CBCFF0FFF  DO          JQMS LREG    MSRA                    WA0              COPY INITIAL X TO FINAL X IF DX < 0.
       AF 7CB8FF1FFF  DO          JQMS LREG    MSRB                    WA1              COPY INITIAL Y TO FINAL Y IF DX < 0.
       B0 7FDEFFFFF0  DO               LADD    MDTF                                F0   BRANCH TO PATCH3
       B1 6FE397173F  DO   FLA         LSAG DE MSRB        RA1 CR1     WA1           C 3F   FIND DY = YF-YI.  SAVE QMSB.
       B2 7CE4F71724  DO          JQMS LSAG DE MSRA            CR1     WA1           C 24   IF DY < 0, MAKE IT + AND SET SLOPE SW.
       B3 6FF487F73F  DO   FLA              DE MSRA        RA0 CR1               C 3F   SAVE MSB OF DX-DY.
       B4 6CB78F1E15  DO   FLA    JQMS LREG DE             RA0         WA1 ZERO    15   IF DX<DY, HEIGHT = DX AND RESET TAN SW.
       B5 7CBCFF0FFF  DO          JQMS LREG    MSRA                    WA0              IF DX<DY, LENGTH=DY.
       B6 7FDEFFFFE9  DO               LADD    MDTF                                E9   BRANCH TO PATCH1.
       B7 AE0C07F7F0  SK N FLA    JZED SLLG    MSRA AMPG RA0 CR1                 C F0   SKIP UNLESS LENGTH = HEIGHT, DOUBLE SRA
       B8 7FDEFFFFBF  DO               LADD    MDTF                                BF   BRANCH TO HEQL.
       B9 7F9FFFFEFF  DO               LSRB                                 ZERO        ZERO SHIFT REGISTER B.
       BA 7FBAFE7FFF  DO               LREG    MFLB                RB6 WA7              SAVE LR.
       BB 6FBF8FEEFF  DO   FLA         LREG                RA0         WB6 ZERO         PUT LENGTH IN FILE B.
       BC 67CAFEFFFF  DO   SRA         LSAD    MFLB                RB6                       DIVIDE HEIGHT
       BD D96F7FFFFF  BK N        JSTC SLIN         AMPG                           FF        BY LENGTH.
       BE 3FB8FF1AFF  SK               LREG    MSRB                    WA1 BMA0    FF   SAVE MS BYTE OF SLOPE AND SKIP.
HEQL   BF 7FB8FF1AFF  DO'              LREG    MPRM                    WA1 BMA0    FF   SET SLOPE TO ALL ONES IF H = L.
       C0 38FFFFFFF1  SK          JMIN                                             F1   SKIP IF ROLL SWITCH SET.
       C1 7FDEFFFFDA  DO               LADD    MDTF                                DA   BRANCH TO ACCUM0.
       C2 7F8FFFFEFF  DO               LSRA                                 ZERO        ZERO SHIFT REGISTER A.
       C3 B89AFFFFF5  SK N        JMIN LSRB    MFLB                RB7             F5   PUT UNROLLED XI IN SRB.  SKIP IF NOT TAN.
       C4 7FDEFFFFC8  DO               LADD    MDTF                                C8   BRANCH TO PTAN.
       C5 67AAFCFFFF  DO   SRA         LSAM    MFLB                RB4                       MULTIPLY XI
       C6 D97F7FFFFF  BK N        JSTC SRAK         AMPG                           FF        BY SIN(PHI).
       C7 7FDEFFFFCA  DO               LADD    MDTF                                CA   BRANCH TO PCOT.
PTAN   C8 67AAFBFFFF  DO   SRA         LSAM    MFLB                RB3                       MULTIPLY XI
       C9 D97F7FFFFF  BK N        JSTC SRAK         AMPG                           FF        BY COS(PHI).
PCOT   CA 193F7FFFF5  AD          JSTC SRAR         AMPG                           F5   SHIFT RIGHT 6X TO JUSTIFY BINARY POINT.
       CB 7FB4FFEF3F  DO               LREG DE MSRA                    WB6         3F   SAVE THIS VALUE & SAVE QMSB.
       CC 7CBCF7E7FF  DO          JQMS LREG    MSRA            CR1     WB6       C      SAVE COMPLEMENT IF NEGATIVE.
       CD 6F9F9FFEFF  DO   FLA         LSRB                RA1              ZERO        PUT SLOPE IN SRB.
       CE 7F8FFFFEFF  DO               LSRA                                 ZERO        ZERO SRA.
       CF 191F7FFFF7  AD          JSTC SRLG         AMPG                           F7   SHIFT RIGHT 8 PLACES.
       D0 [illegible] DO   SRA         LSAM    MFLB                RB6                       MULTIPLY SLOPE
       D1 [illegible] [illegible] JSTC SRAK         AMPG                           FF        BY SAVED VALUE.
       D2 [illegible] DO   FLA         LREG                [illegible]  WB6 ZERO            RESTORE LR.
       D3 [illegible] DO               LSRA    MFLB                [illegible] BMA0 [illegible]   PUT MSB OF INITIAL UNROLLED X IN SRA.
       D4 67F2FBFF3F  DO   SRA              DE MFLB                [illegible]     [illegible]   [illegible]
       D5 7C8EFFFC7F  DO          JQMS LSRA    MDTF                         BMRA   [illegible]   IF QMSB=1, [illegible]
       D6 648BF7F7FF  DO   SRA    JQMS LSRA    MSRB            CR1               C      IF QMSB=1, SUBTRACT [illegible]
       D7 FC8EFFFC80  DO N        JQMS LSRA    MDTF                         BM0A   80   IF QMSB=0, PUT X [illegible]
       D8 E48BFFFFFF  DO N SRA    JQMS LSRA    MSRB                                     IF QMSB=0, ADD SRB TO ACC.
       D9 6FBC9F1CFF  DO   FLA         LREG    MSRA        RA1         WA1 BM0A    FF   COMBINE SLOPE AND ACCUM.
ACCUM0 DA 6F8EDFFA60  DO   FLA         LSRA    MDTF        RA5              BMA0   60   PUT XI+X'6000' IN SRA.
       DB 191F7FFFF7  AD          JSTC SRLG         AMPG                           F7   SHIFT RIGHT 8 PLACES.
       DC 6F9EEFFAA0  DO   FLA         LSRB    MDTF        RA6              BMA0   A0   PUT YI+X'A000' IN SRB.
       DD 67BBFF5AFF  DO   SRA         LREG    MSRB                    WA5 BMA0    FF   COMBINE & SAVE YI & XI.
       DE 6F8F8FFEFF  DO   FLA         LSRA                RA0              ZERO        PUT LENGTH IN SRA.
       DF 193F7FFFF6  AD          JSTC SRAR         AMPG                           F6   SHIFT RIGHT 7 PLACES.
```

```
NAME   AD   OBJECT     AV N AMX Z SKIP SHFT  DX MMUX ADMX FLA CRY FLB FWT  MASK  C DA
       E0 7FBCFFFFFF DO                LREG     MSRA                  WB7                  PUT SHIFTED LENGTH IN FILE B.
       E1 6F9F9FFEFF DO    FLA         LSRB                     RA1            ZERO        PUT SLOPE/ACC IN SRB.
       E2 7FF7DFFF40 DO                     DE                  RA5      RB7               40 ADVANCE LIST.
       E3 7FFFDFFFFF DO                                         RA5      RB7               NO-OP.
       E4 7FFFDFFFFF DO                                         RA5      RB7               NO-OP.
       E5 7FDAF8FFFF DO                LADD     MFLB                CR1 RB0               RETURN TO CALLING PROGRAM.
PALPH  E6 6F8F8F1EFF DO    FLA         LREG                     RA0            WA1 ZERO    PUT ALPHA IN SLOPE POS.  ZERO ACC.
       E7 7FBEFF0A03 DO                LREG     MDTF                           WA0 BMA0  03 SET LENGTH.
       E8 7FDEFFFFDA DO                LADD     MDTF                                     DA BRANCH TO ACCUMO.
PATCH1 E9 6F8F97FEFF DO    FLA         LSRA                     RA1 CR1            ZERO     PUT HEIGHT+1 IN SRA.
       EA 6FBE8F0A01 DO    FLA         LREG     MDTF            RA0            WA0 BMA0  01 INCREMENT LENGTH
       EB 7FDEFFFFB7 DO                LADD     MDTF                                     B7 RETURN FROM PATCH1
PATCH2 EC AEF827F718 SK N FLA   JZED            MPRM AMPG RA2 CR1                    C 18 SKIP IF THETAQ-7 IS NOT ZERO
       ED 7FDEFFFF35 DO                LADD     MDTF                                     35 BRANCH TO HORIZ.
       EE 4EF827F70E BK    FLA   JZED            MPRM AMPG RA2 CR1                    C 0E BACK UP IF THETAQ-187 = ZERO
       EF 7FDEFFFF21 DO                LADD     MDTF                                     21 RETURN FROM PATCH2.
PATCH3 F0 6F8FDFFEFF DO    FLA         LSRA                     RA5                ZERO     RELOAD START X IN SRA
       F1 6F9FEFFEFF DO    FLA         LSRB                     RA6                ZERO     RELOAD START Y IN SRB
       F2 6FB4870714 DO    FLA         LREG  DE MSRA            RA0 CR1       WA0        C 14 FIND DX = XF-XI.  RESET SLOPE SWITCH.
       F3 7FDEFFFFB1 DO                LADD     MDTF                                     B1 RETURN FROM PATCH3.
       FF FFFFFFFFFF
```

APPENDIX C

FLOWCHART OF DISPLAY PROCESSOR OPERATIONAL PROGRAM

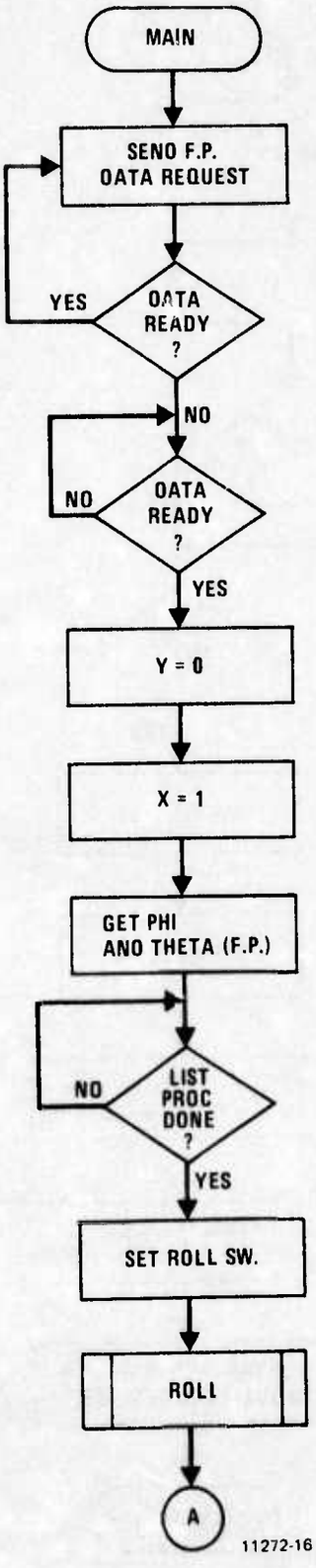

Figure C-1. Flowchart of display processor operational program (sheet 1 of 15)

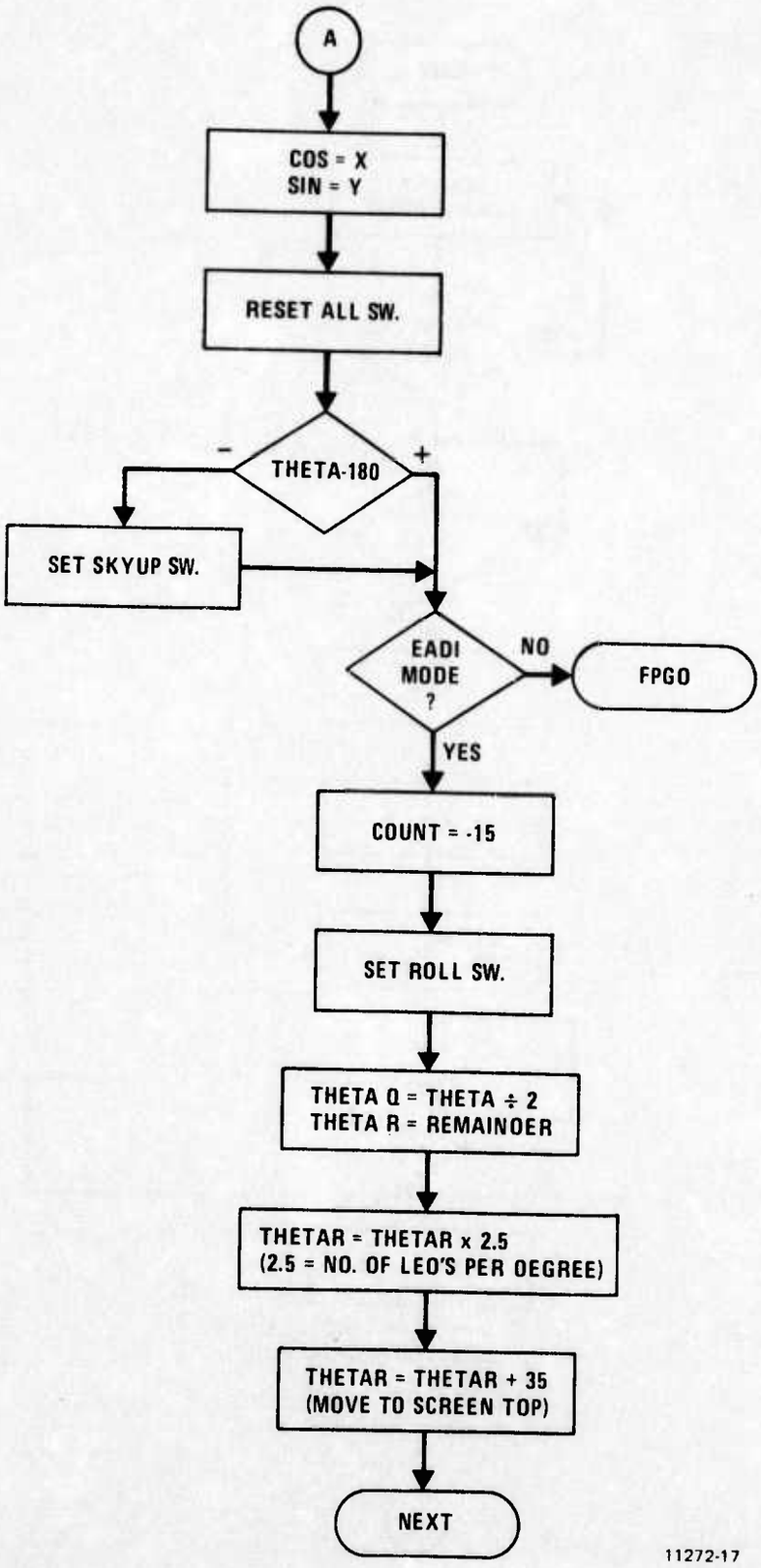

Figure C-1. Flowchart of display processor operational program (sheet 2 of 15)

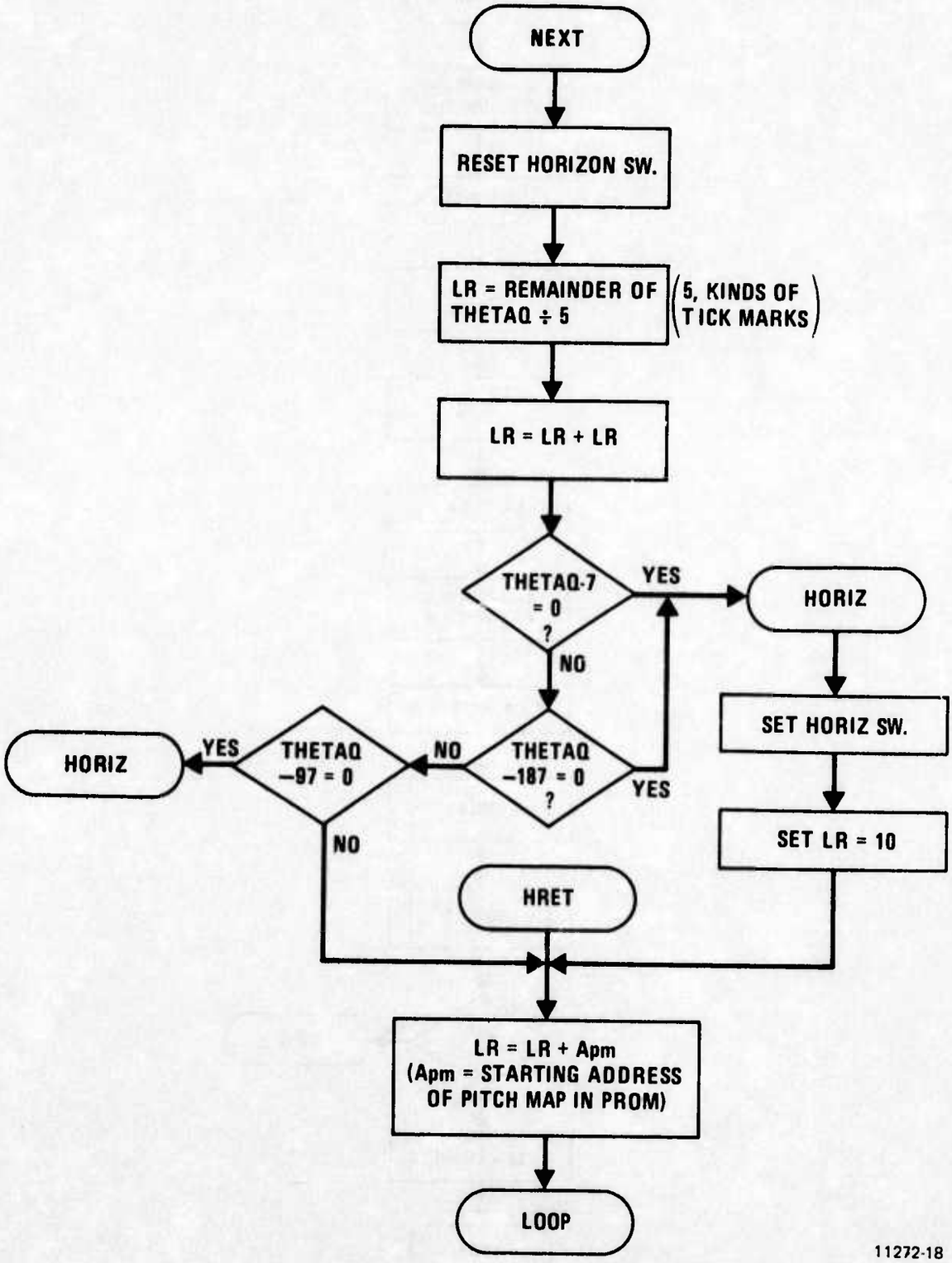

Figure C-1. Flowchart of display processor operational program (sheet 3 of 15)

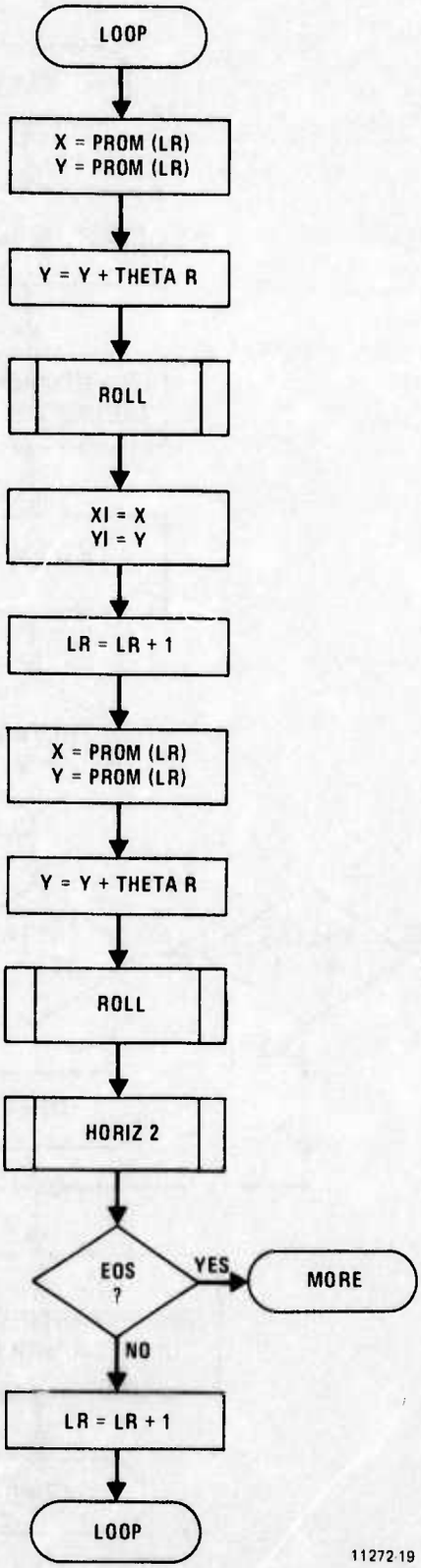

Figure C-1. Flowchart of display processor operational program (sheet 4 of 15)

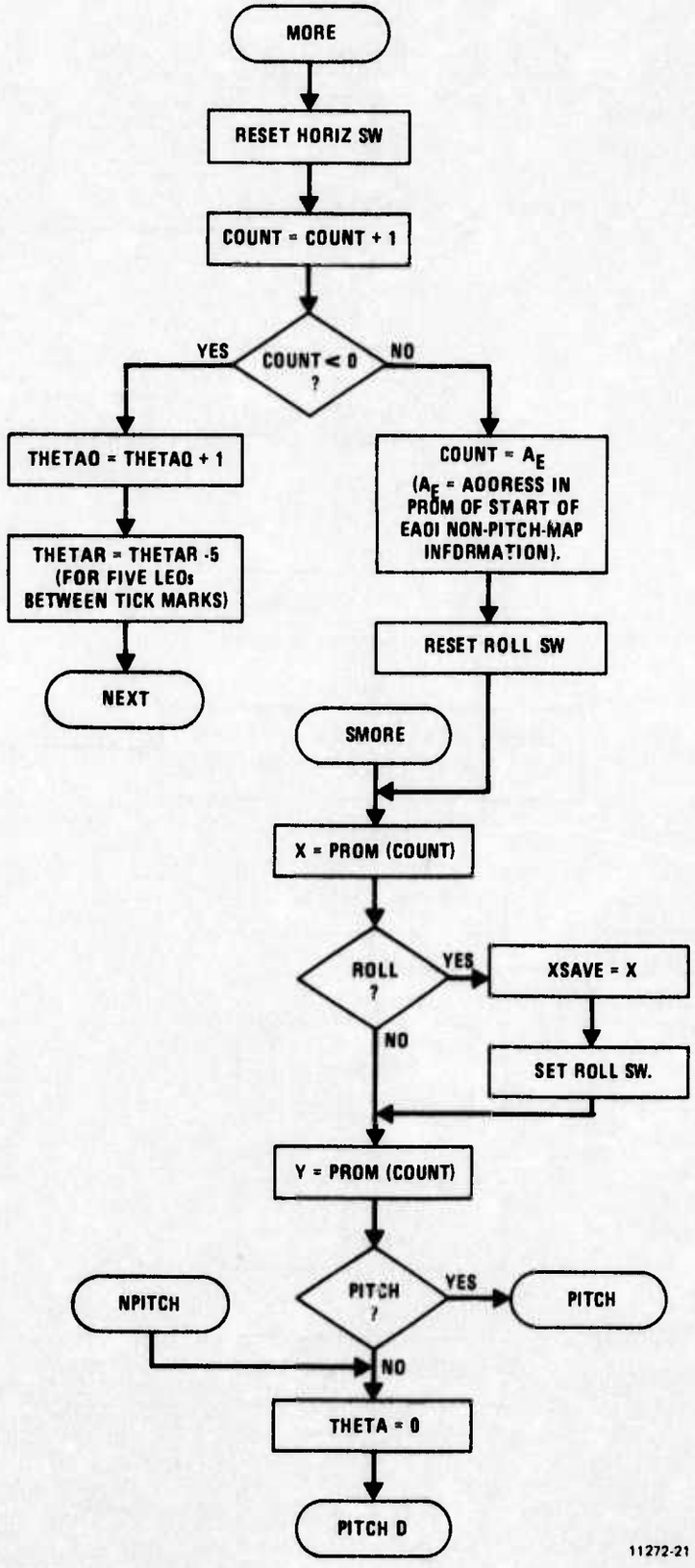

Figure C-1. Flowchart of display processor operational program (sheet 5 of 15)

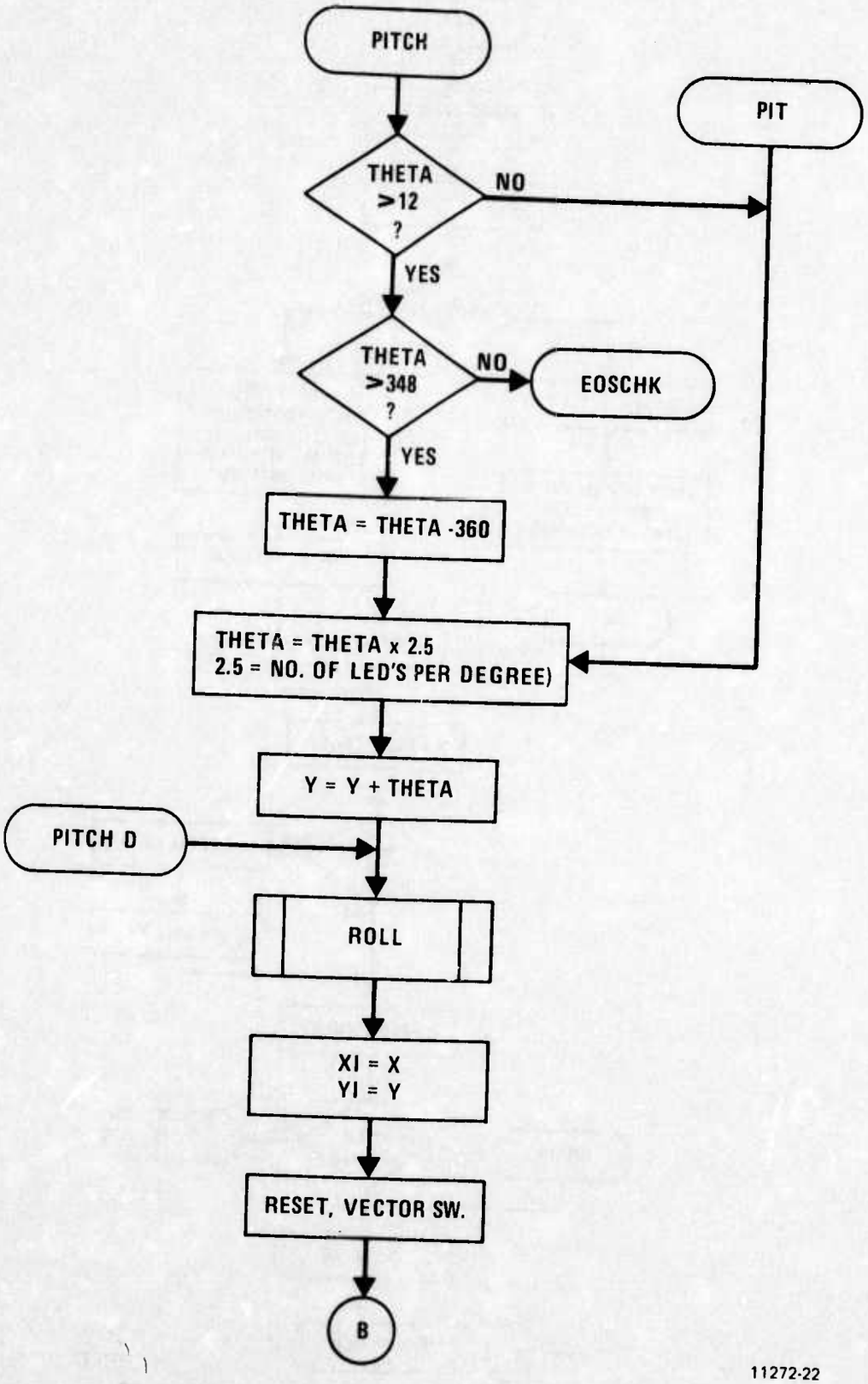

Figure C-1. Flowchart of display processor operational program (sheet 6 of 15)

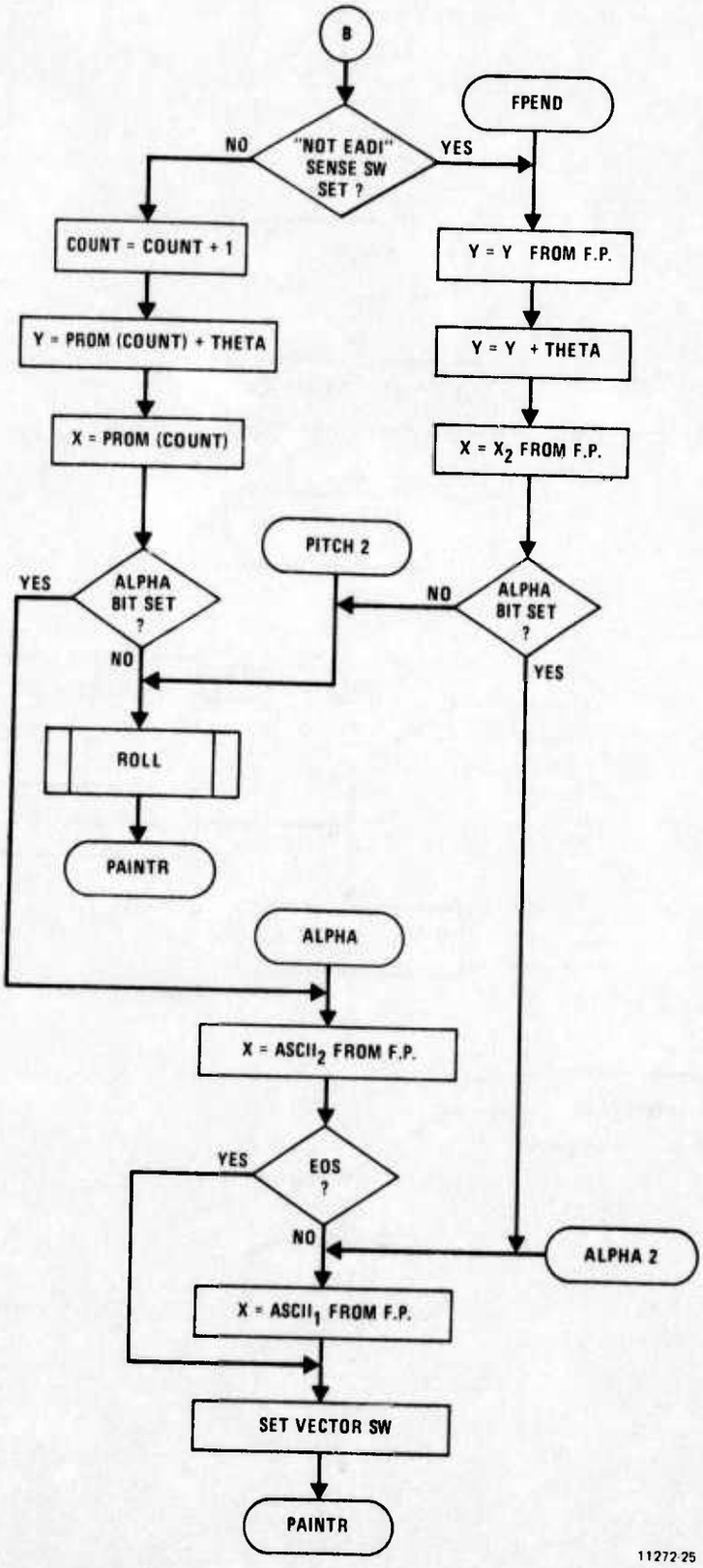

Figure C-1. Flowchart of display processor operational program (sheet 7 of 15)

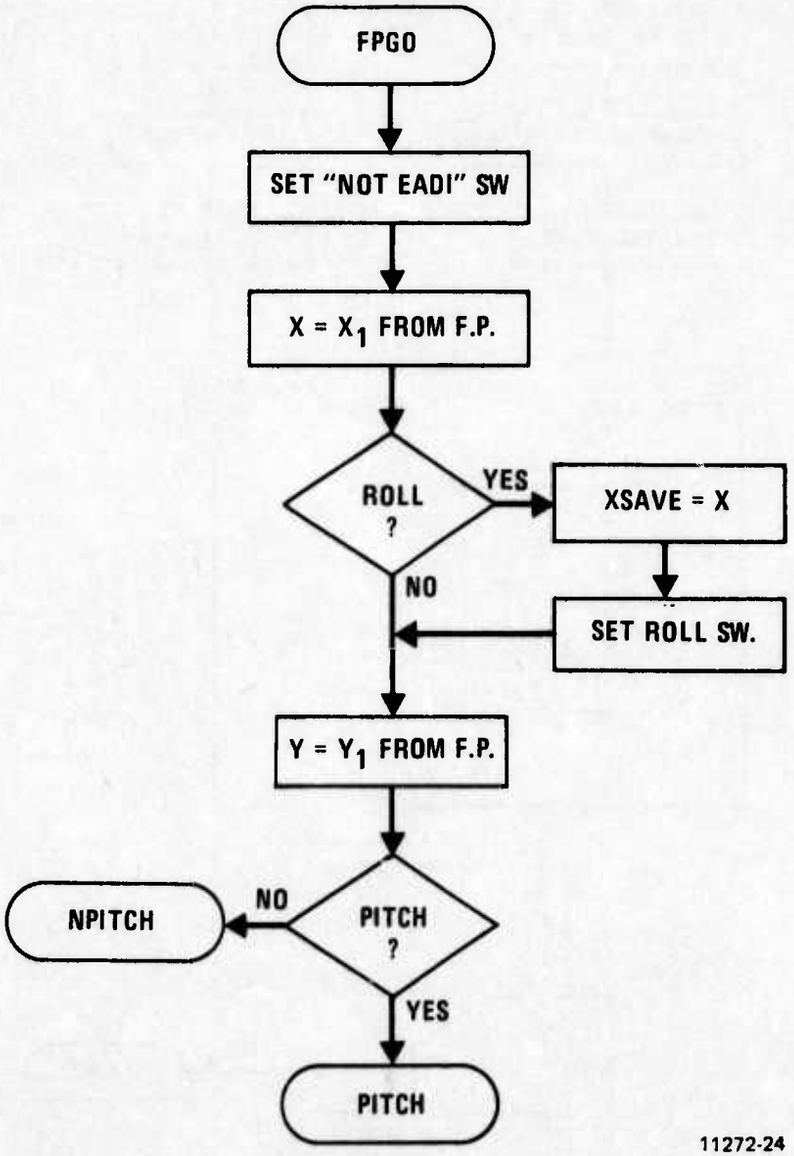

Figure C-1. Flowchart of display processor operational program (sheet 8 of 15)

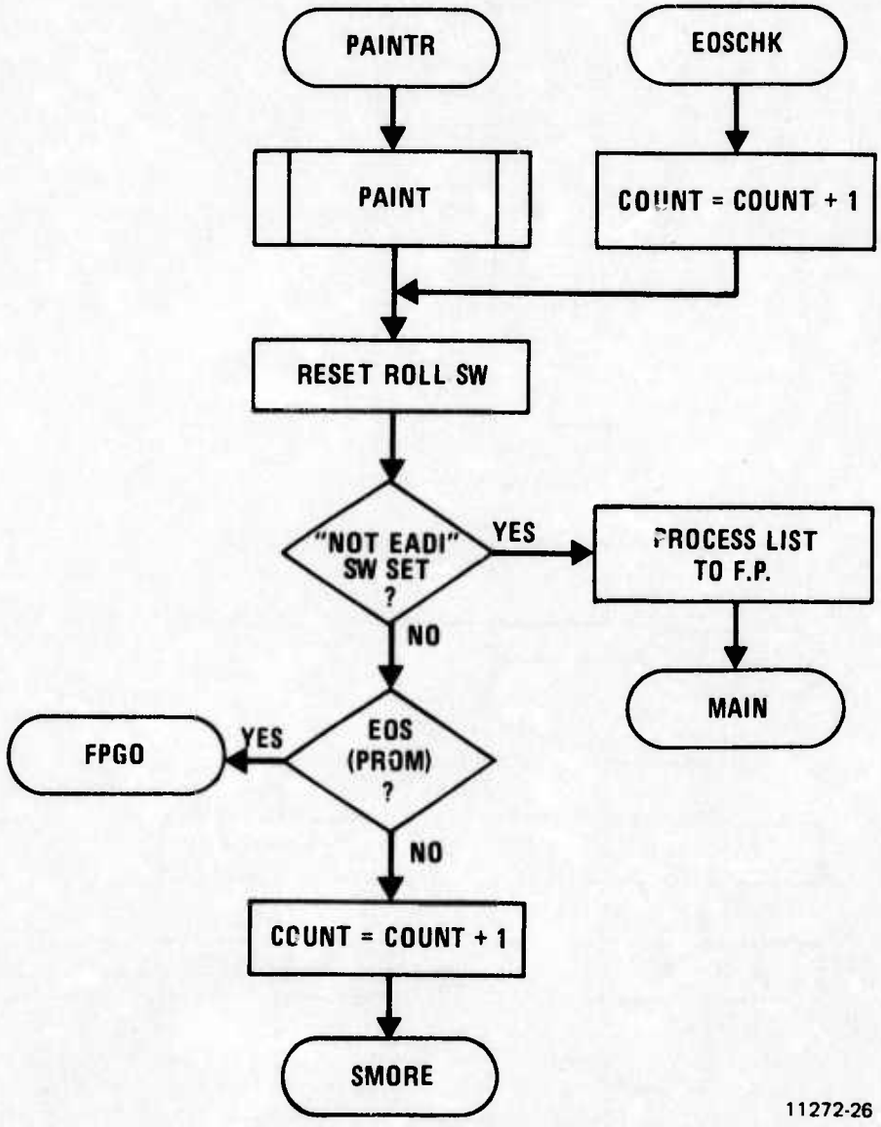

Figure C-1. Flowchart of display processor operational program (sheet 9 of 15)

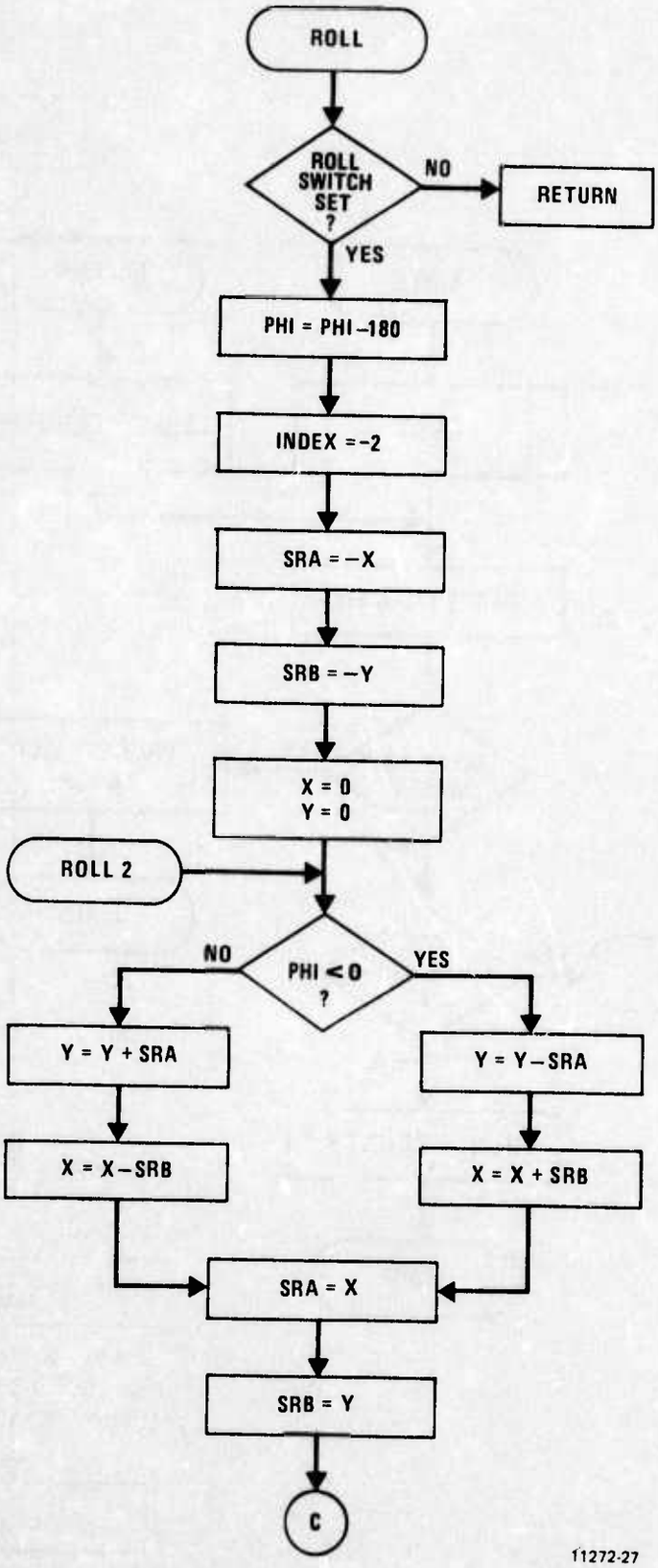

Figure C-1. Flowchart of display processor operational program (sheet 10 of 15)

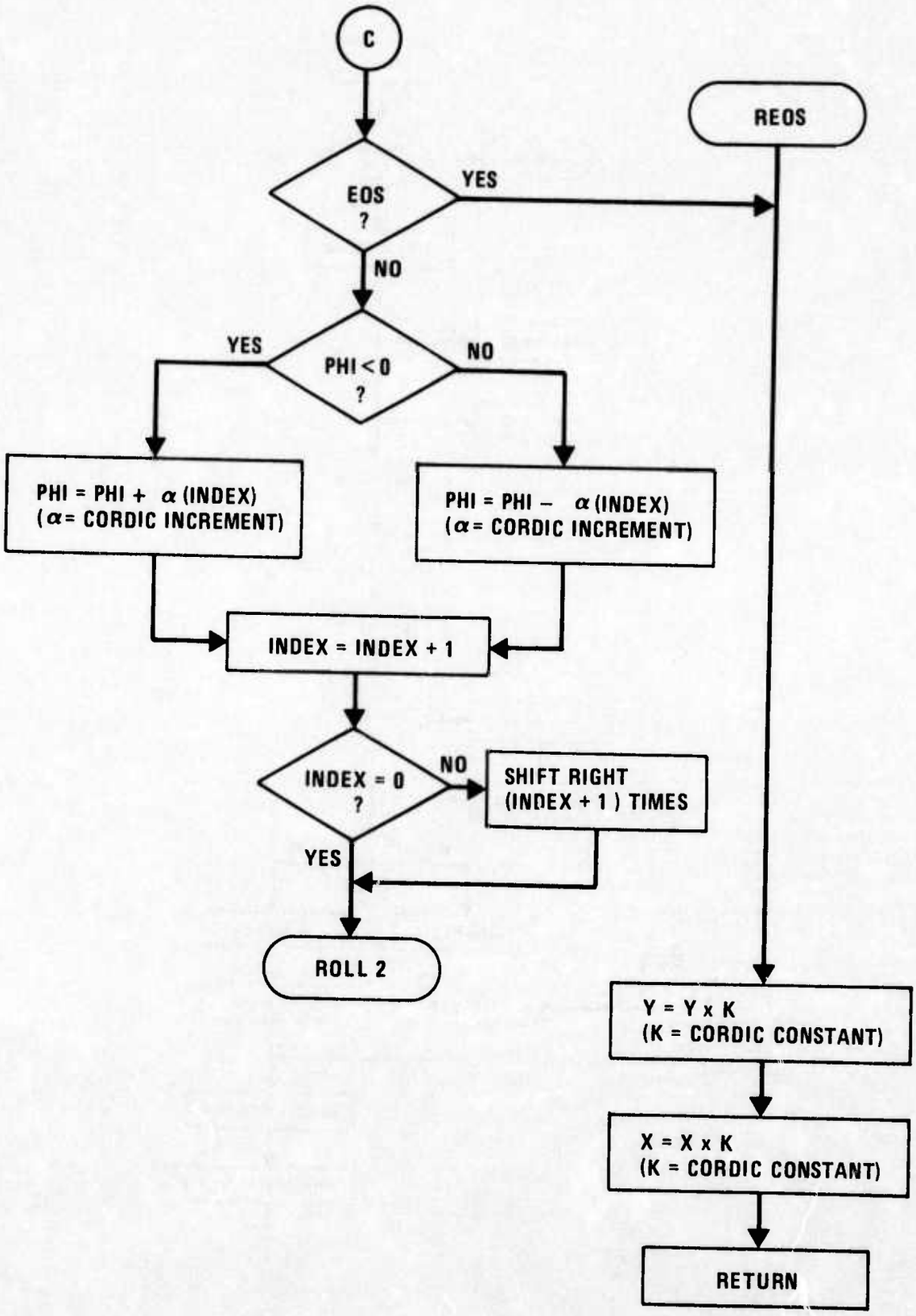

Figure C-1. Flowchart of display processor operational program (sheet 11 of 15)

11272-28

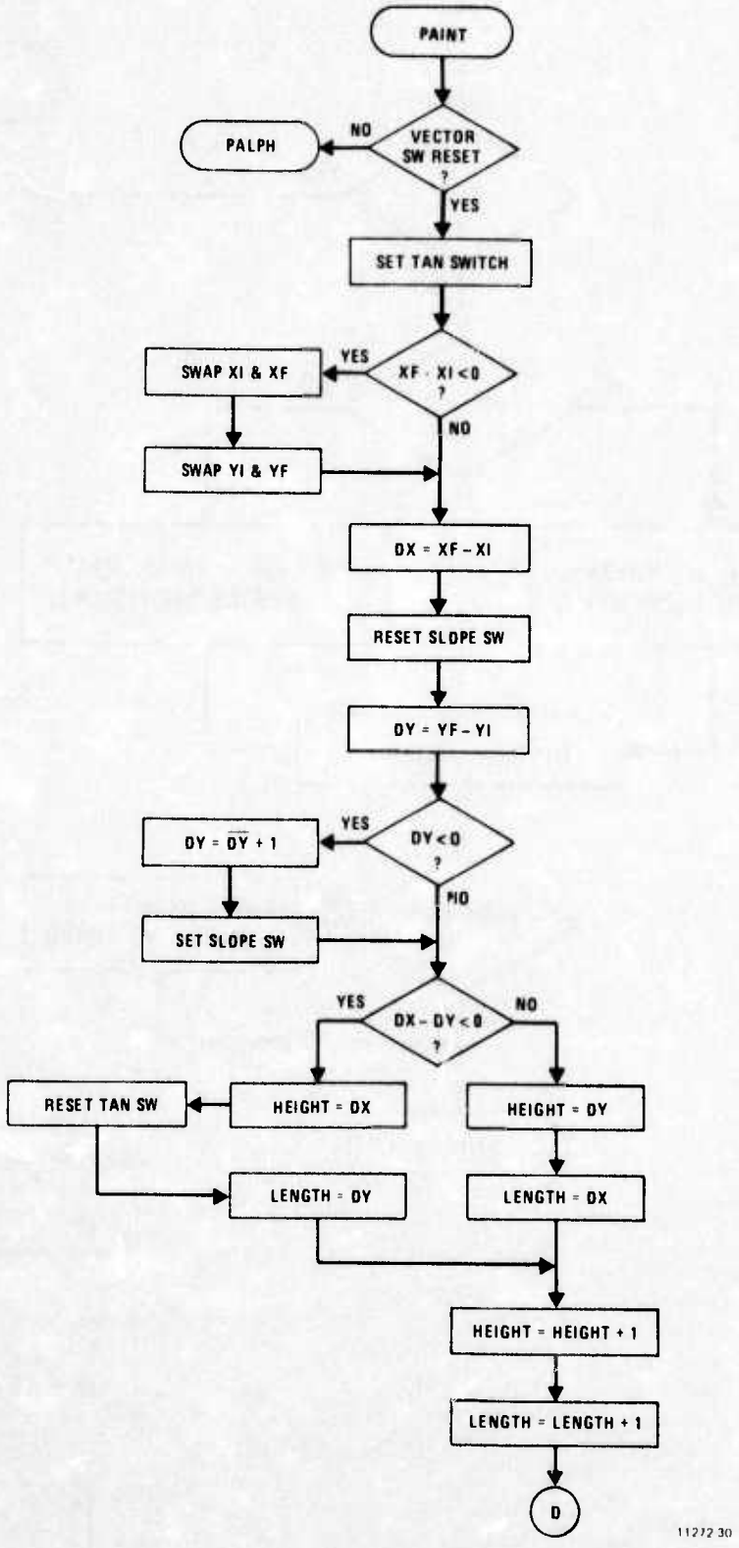

Figure C-1. Flowchart of display processor operational program (sheet 12 of 15)

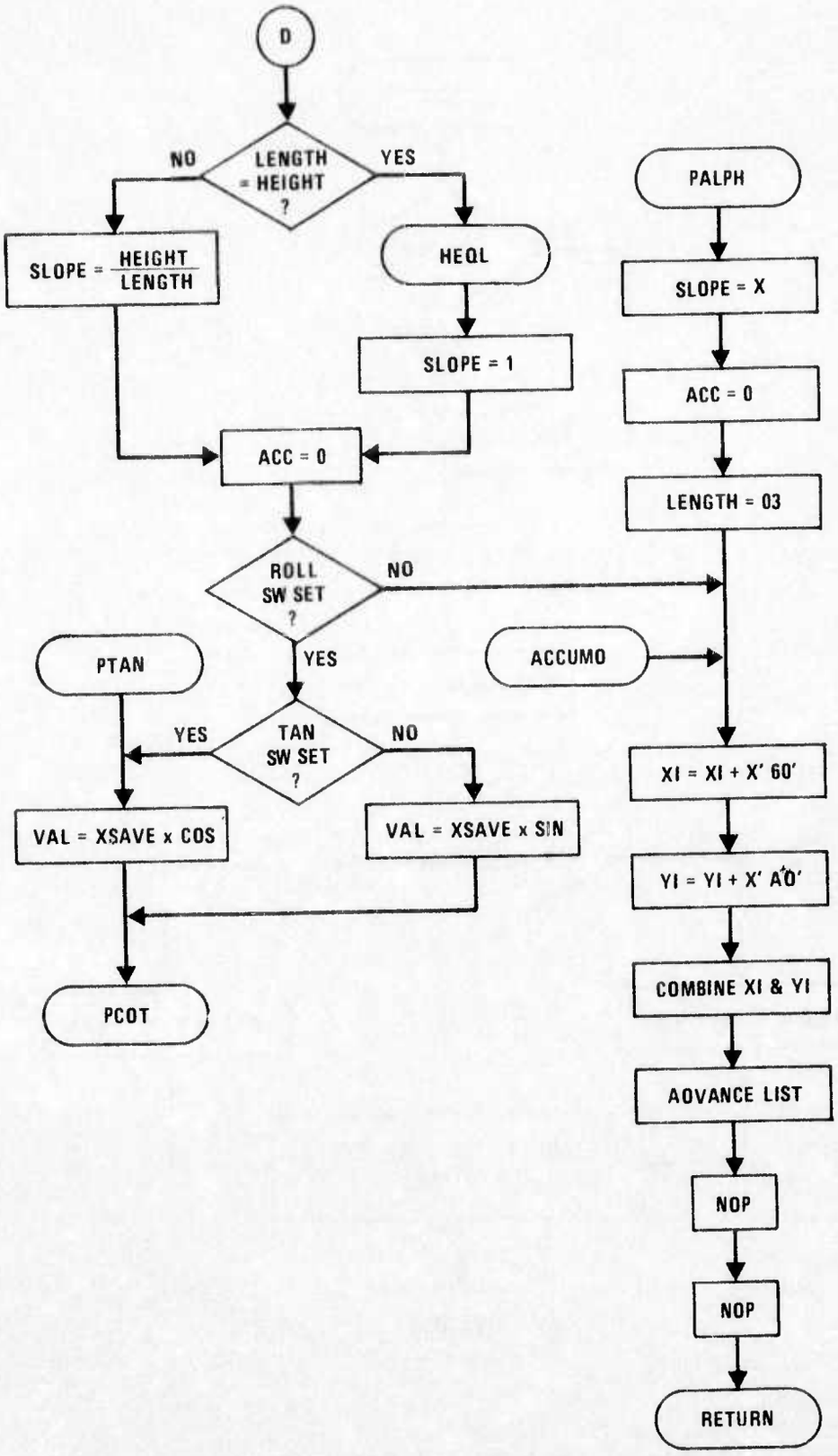

Figure C-1. Flowchart of display processor operational program (sheet 13 of 15)

11272-33

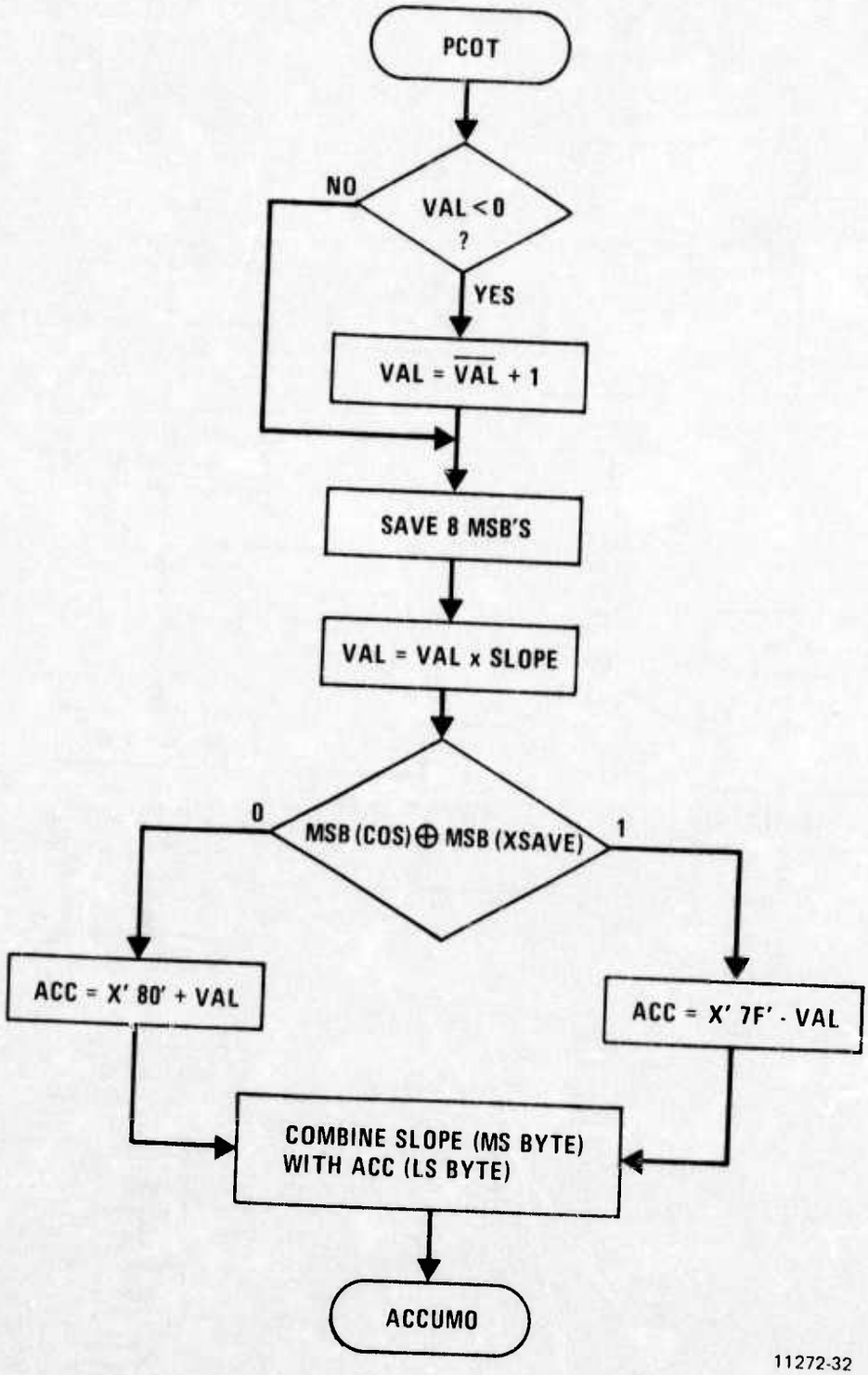

Figure C-1. Flowchart of display processor operational program (sheet 14 of 15)

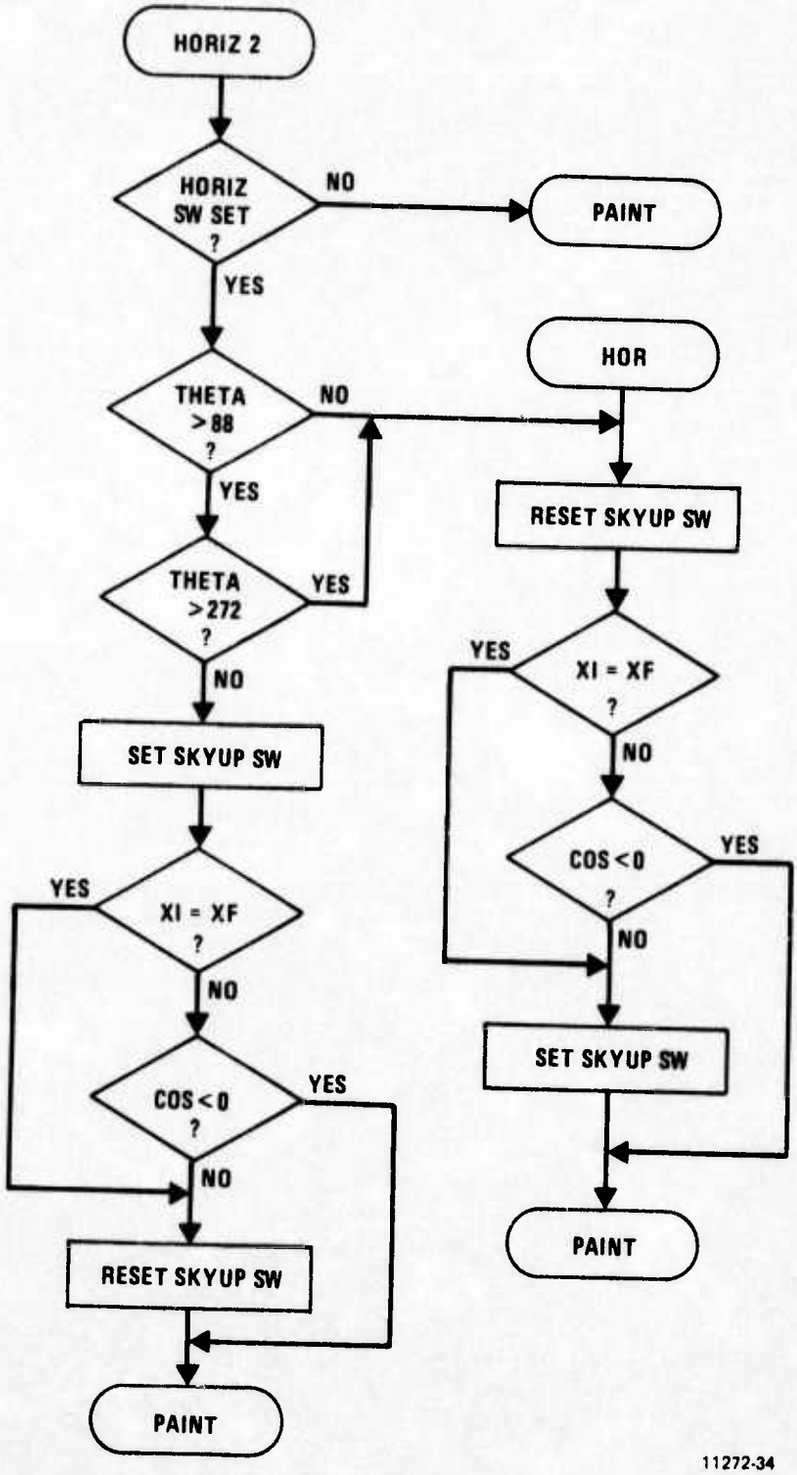

Figure C-1. Flowchart of display processor operational program (sheet 15 of 15)

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